**Summary**

Intel's 3D LUT IP provides an efficient solution for video-colour space conversions and conversion between nonlinear gamuts, and can also offer many other capabilities such as; sepia, black-and-white, vivid colour, the ability to change the colour of specific coloured objects, and to create chroma keys. The 3D LUT IP cleverly uses linear interpolations; either Trilinear or Tetrahedral, or can switch seamlessly between each via an AXI4-Lite control interface. The IP block uses the most significant bits (MSBs) of the 3 colour component inputs to retrieve data values from the contents of the LUT, and the least significant bits (LSBs) to interpolate the final output value. This is demonstrated in the block diagram above.

The interpolation processes used in the 3D LUT IP can be implemented using a relatively small number of gates and memory compared with a non-interpolated 3D LUT enabling implementation of this type of technology on an Intel Field Programmable Gate Array (FPGA), which makes for a more cost-effective solution. Using industry standard interfaces such as AXI4-Streaming and AXI4-Lite enables the IP to be easily integrated into your own Intel FPGA design.

**Applications**

The applications of Intel's 3D LUT IP include:
- Colour Space Conversions
- Chroma Keying
- Dynamic Range Conversions
- Artistic Effects (e.g. sepia, hue rotation, colour volume adjustments)

**Additional Requirements**

The 3D LUT requires an FPGA with AXI4-Streaming Video buses and an AXI4-Lite bus to control the IP and to load new tables.
Key Features

- Colour space converter / colour correction
- Conversion between nonlinear gamuts
- Dynamic range conversion
- Low FPGA resource required
- Support for 4K at 60fps running at 300MHz with 2 pixels per clock and has a scalable support for rates beyond this by increasing pixels per clock. Extendable to 8K
- Support for 8, 10, 12 and 16 bit colour component
- Support for $17^3$, $33^3$ and $65^3$ lookup tables (LUT)
- Supports 3 and 4 output channels from the LUT
- Independently set input / output pixels depth
- Support for Tetrahedral and/or Trilinear interpolation
  If both are enabled there is support for hitless switching between them
- Dynamic update of table values with optional double buffering to enable clean switching to a new LUT data set
- Ability to set LUT precision
- Can accept all major industry standard file formats

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Intel provides a large range of complementary and modular in-house IP cores for video processing and connectivity. These IP cores can be used to create complete solutions for applications in Broadcast, ProAV, Aerospace/Defense, Medical, Automotive and more.

You can get more information on available video IP at www.intel.com/fpga-broadcast or contact an Intel sales representative for further inquiries.

Reference Design

*Is this correct?* Arria 10 SoC Development kit. Fully compatible with Intel ISP, Warp and IP Cores, for more information see the previous section.

3D LUT Example Results

In the images displayed below, you will notice the differing outputs available from the 3D LUT when different values are loaded.

![Figure 2. Original](image1.png)
![Figure 3. Increased saturation](image2.png)
![Figure 4. Increased brightness](image3.png)

![Figure 5. Hue rotate](image4.png)
![Figure 6. Hue rotate](image5.png)
![Figure 7. No saturation](image6.png)