82599

10 GBE PCIE* V2.1 (5GT/S) DUAL PORT ETHERNET CONTROLLER REFERENCE DESIGN

PAGE INDEX

PIN NAMING CONVENTION

NC... - PIN IS NOT CONNECTED IN THE PACKAGE
RSVD..._NC - RESERVED PIN. SHOULD BE LEFT UNCONNECTED.
RSVD..._VSS - RESERVED PIN. SHOULD BE CONNECTED TO GROUND.

DISCLAIMER: THIS REFERENCE SCHEMATIC IS NOT INTEDED TO BE USED AS A STAND ALONE OR PRODUCTIZABLE DESIGN

LAN ACCESS DIVISION
2111 N.E. 25th AVENUE
HILLSBORO, OR 97124

TITLE	SIZE	CODE	DOCUMENT NUMBER	REV	DATE	SHEET
82599 - REFERENCE SCHEMATIC	B			2.3	07/25/2012	1

FUNCTIONAL BLOCK DIAGRAM

25 MHZ CRYSTAL CIRCUIT
OR
25 MHZ OSCILLATOR
PECL OR CML DIFFERENTIAL OSC.

THIS SCHEMATIC SHOWS ONLY A FEW POSSIBLE CONFIGURATIONS.
CHOOSING THE RIGHT IMPLEMENTATION IS APPLICAION SPECIFIC AND
IS THE RESPONSABILITY OF THE SYSTEM DESIGNER.

HOST

PCIE V2.0 (5GT/S)
X8 LINK

82599

10 GBE CONTROLLER

SMBUS &
NC-SI INTERFACE

JTAG INTERFACE

EEPROM

FLASH

MAUI I/F

MDIO I/F

I2C I/F

SDPS & LEDS

PORT 0

SFP+ OPTICAL SOLUTION
SCHEMATIC SHOWS SFI CONNECTIVITY TO AN SFP+ CAGE
AND THE CONNECTION CAN BE OPTICAL OR DIRECT ATTACH
TWINAX CABLE

MAUI I/F

MDIO I/F

I2C I/F

SDPS & LEDS

PORT 1

XAUI/KX/KX4/KR BACKPLANE SOLUTION
SCHEMATIC SHOWS SIMPLE CONNECTIVITY THROUGH
AN HM-ZD BACKPLANE CONNECTOR (ATCA ZONE-2 J23).
FOR KX AND KR ONLY LANE 0 IS BEING USED.

CX4 SOLUTION
SCHEMATIC SHOWS SIMPLE CONNECTIVITY TO A REGULAR
CX4 CONNECTOR.

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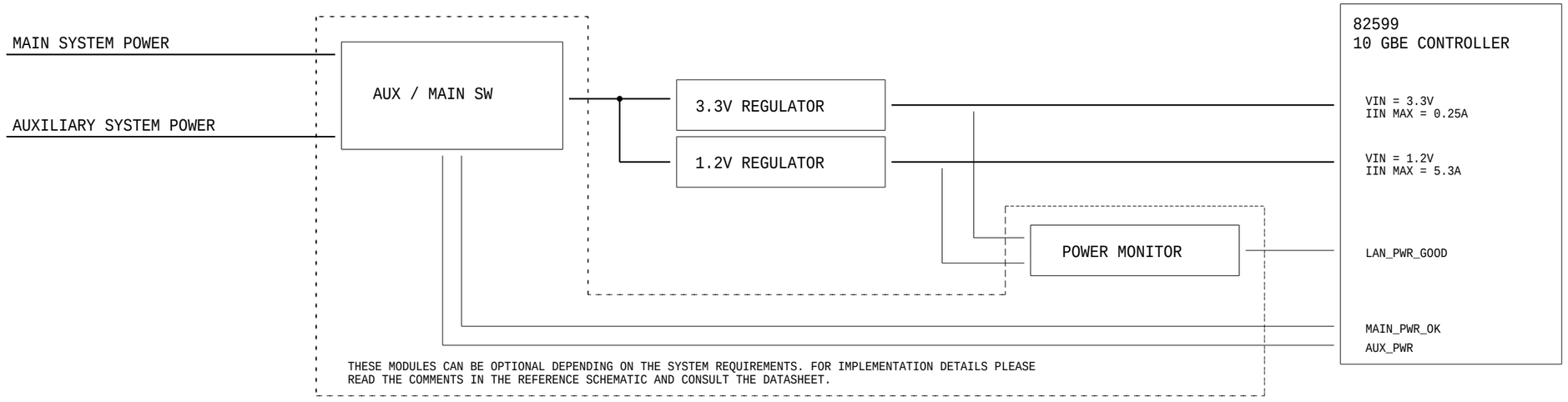
POWER SUPPLY BLOCK DIAGRAM



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ROUTE AS 85 OHM DIFFERENTIAL PAIRS.
TRACES WITHIN A PAIR MUST BE MATCHED
WITHIN 5 MILS. PAIR TO PAIR TRACE
LENGTHS SHOULD BE MATCHED WITHIN 1 INCH
WITH EXCEPTION OF PCIE REFERENCE CLOCK.

FOR MORE GUIDELINES SEE DATASHEET.

U1
82599

IN	PER_0_N	AC21	PER_0_n	PCI EXPRESS RECEIVE	
IN	PER_0_P	AC20	PER_0_p		
IN	PER_1_N	AA21	PER_1_n		
IN	PER_1_P	AA20	PER_1_p		
IN	PER_2_N	U21	PER_2_n		
IN	PER_2_P	U20	PER_2_p		
IN	PER_3_N	R21	PER_3_n		
IN	PER_3_P	R20	PER_3_p		
IN	PER_4_N	K21	PER_4_n		
IN	PER_4_P	K20	PER_4_p		
IN	PER_5_N	H21	PER_5_n		
IN	PER_5_P	H20	PER_5_p		
IN	PER_6_N	D21	PER_6_n		
IN	PER_6_P	D20	PER_6_p		
IN	PER_7_N	B21	PER_7_n		
IN	PER_7_P	B20	PER_7_p		
IN	PE_CLK_N	AB24	PE_CLK_n		
IN	PE_CLK_P	AB23	PE_CLK_p		
OUT/IN	PE_WAKE_N	AA18	PE_WAKE_N		
	PE_RST_N	AD18	PE_RST_N		
	PE_RBIAS	M24	PE_BIAS		
		N24	PE_RSENSE		

	PET_0_n	Y24	PET_0_AC_N	0.1UF X7R 0402LF C27	PET_0_N	OUT
	PET_0_p	Y23	PET_0_AC_P	0.1UF C28	PET_0_P	OUT
	PET_1_n	V24	PET_1_AC_N	0.1UF X7R 0402LF C29	PET_1_N	OUT
	PET_1_p	V23	PET_1_AC_P	0.1UF X7R 0402LF C30	PET_1_P	OUT
	PET_2_n	T24	PET_2_AC_N	0.1UF X7R 0402LF C31	PET_2_N	OUT
	PET_2_p	T23	PET_2_AC_P	0.1UF X7R 0402LF C32	PET_2_P	OUT
	PET_3_n	P24	PET_3_AC_N	0.1UF X7R 0402LF C33	PET_3_N	OUT
	PET_3_p	P23	PET_3_AC_P	0.1UF X7R 0402LF C34	PET_3_P	OUT
	PET_4_n	J24	PET_4_AC_N	0.1UF X7R 0402LF C35	PET_4_N	OUT
	PET_4_p	J23	PET_4_AC_P	0.1UF X7R 0402LF C36	PET_4_P	OUT
	PET_5_n	G24	PET_5_AC_N	0.1UF X7R 0402LF C37	PET_5_N	OUT
	PET_5_p	G23	PET_5_AC_P	0.1UF X7R 0402LF C38	PET_5_P	OUT
	PET_6_n	E24	PET_6_AC_N	0.1UF X7R 0402LF C39	PET_6_N	OUT
	PET_6_p	E23	PET_6_AC_P	0.1UF X7R 0402LF C40	PET_6_P	OUT
	PET_7_n	C24	PET_7_AC_N	0.1UF X7R 0402LF C41	PET_7_N	OUT
	PET_7_p	C23	PET_7_AC_P	0.1UF X7R 0402LF C42	PET_7_P	OUT

PCI EXPRESS TRANSMIT

ROUTE AS 85 OHM DIFFERENTIAL PAIRS
TRACES WITHIN A PAIR MUST BE MATCHED
WITHIN 5 MILS. PAIR TO PAIR TRACE
LENGTHS SHOULD BE MATCHED WITHIN 1 INCH.

FOR MORE GUIDELINES SEE DATASHEET.

PLACE CAPACITORS
CLOSE TO PCIE
TRANSMITTER.

JRST_N	B14	JRST_N	
JTCK	B16	JTCK	
JTMS	B13	JTMS	
JTDI	A13	JTDI	
JTDO	B15	JTDO	

JTAG

IC

3P3V_NIA

R1 100K 0402LF

1P2V_NIA

R38 24.90 0.5% 0402LF

PLACE CLOSE TO 82599. TOTAL
PE_RBIAS/PE_RSENSE TRACE LENGTH
SHOULD BE LESS THAN 1 INCH.

JTAG HEADER:
RECOMMENDED FOR DEBUG PURPOSES
TO BE USED WITH JTAG TO USB ADAPTER

J4
SCONN6_966926_3

JRST_N	1	2	JTMS	
JTDO	3	4		
JTDI	5	6	JTCK	

SMLF CONN

GND

(SAMTEC TMM-103-01-L-D-SM OR EQUIVALENT CONN)

3P3V_NIA

R41 8.2K 0402LF

R42 8.2K 0402LF

R70 3.3K 0402LF

R39 470 0402LF

GND

R40 470 0402LF

GND

NOTE:
JRST_N HAS INTERNAL PULL UP
REMOVE R40 FOR UTAG ACCES
TO 82599

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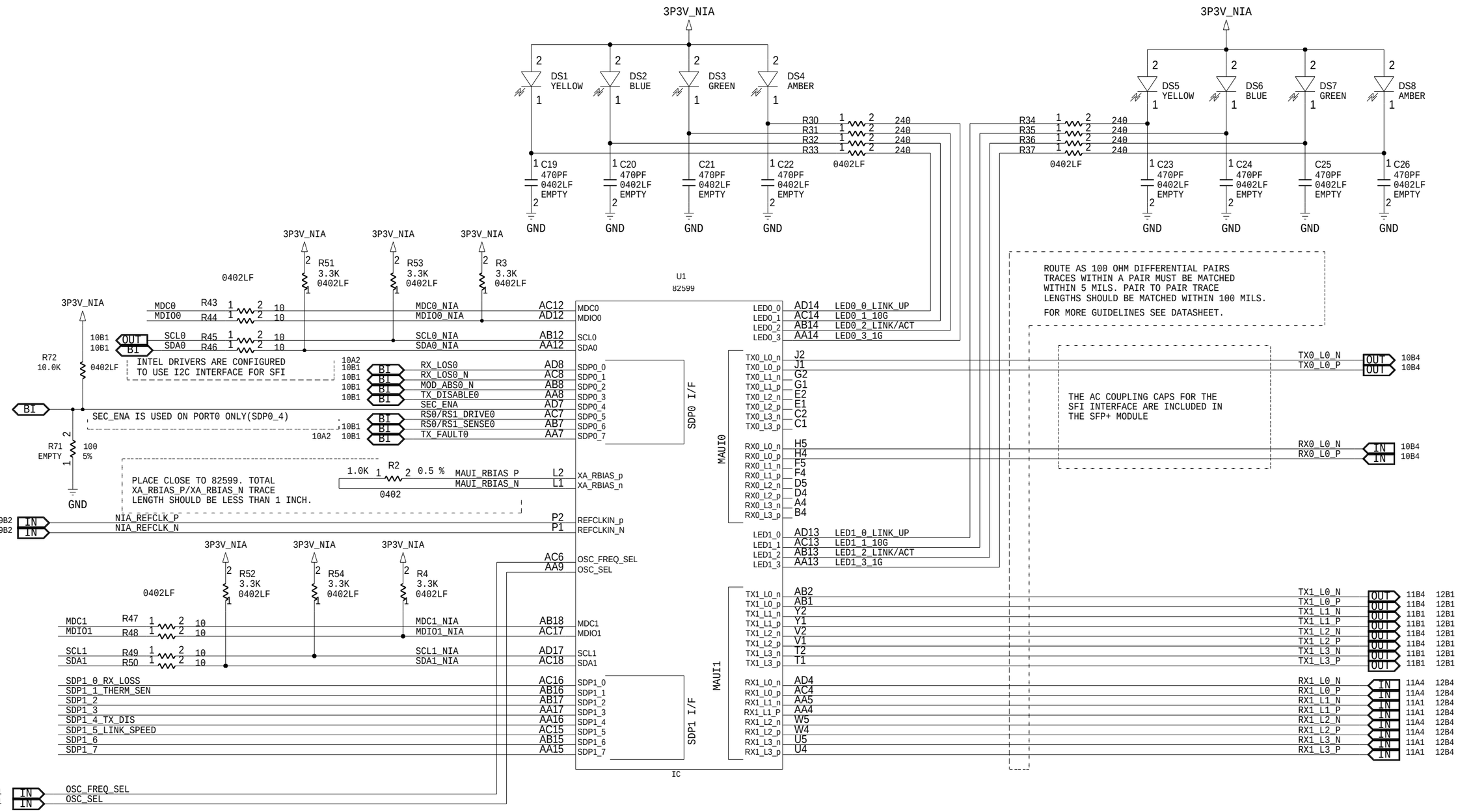

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82599 - REFERENCE SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.3	DATE 07/25/2012	SHEET 5

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IF SM_BUS IS NOT USED,SMB_CLK AND
SMB_DAT STILL NEED TO BE PULLED UP TO 3.3V

3P3V_NIA

R55 8.2K 0402LF
R56 8.2K 0402LF
R57 8.2K 0402LF
R58 8.2K 0402LF
R7 8.2K 0402LF
R9 8.2K 0402LF
R11 8.2K 0402LF
R13 8.2K 0402LF

U1
82599

IN	NCSI_CLK_IN	AC11	NCSI_CLK_IN	NCSI
OUT	NCSI_CRS_DV	AB11	NCSI_CRS_DV	
IN	NCSI_TX_EN	AB10	NCSI_TX_EN	
IN	NCSI_TXD_0	AA10	NCSI_TXD_0	
IN	NCSI_TDX_1	AD11	NCSI_TXD_1	
OUT	NCSI_RXD_0	AA11	NCSI_RXD_0	
OUT	NCSI_RXD_1	AC10	NCSI_RXD_1	
6A4 6A4 OUT	SMBALRT_N	AA19	SMBALRT_N	SMB
6A4 6A4 B1	SMBCLK	AC19	SMBCLK	
6A4 6A4 B1	SMBDAT	AB19	SMBD	
IN	LAN0_DIS_N	AD21	LAN0_DIS_N	
IN	LAN1_DIS_N	AD20	LAN1_DIS_N	
	MAIN_PWR_OK	AC9	MAIN_PWR_OK	
	AUX_PWR	AB9	AUX_PWR	
	POR_BYPASS	D19	POR_BYPASS	
	LAN_PWR_GOOD	A14	LAN_PWR_GOOD	

IC

IF THE DESIGN DOESN'T WANT TO USE THE
INTERNAL POR CIRCUIT AN EXTERNAL RESET
SIGNAL: LAN_PWR_GOOD CAN BE USED.
TO BYPASS THE INTERNAL POR CIRCUIT PULL
POR_BYPASS HIGH.

FOR MORE DETAIL PLEASE CONSULT THE DATASHEET.

R5 100 0402LF
R6 100 0402LF
R8 10.0K 5% 0402LF
R10 10.0K 5% 0402LF
R12 10.0K 5% 0402LF

GND

IF THE IMPLEMENTATION RELIES ON A LAN CONECTION IN LOW POWER STATES
AND CHANGES THE POWER SUPPLY FROM THE MAIN RAIL TO THE AUX RAIL
ON THE FLY, THEN USING THE MAIN_PWR_OK SIGNAL, THE POWER SUPPLY HAS
TO SIGNAL THE 82599 CONTROLLER WHICH RAIL IS SUPPLYING ITS POWER.
IN THIS CASE AUX_PWR HAS TO BE PULLED HIGH TOO.

FOR MORE DETAIL PLEASE CONSULT THE DATASHEET.

SERIAL EEPROM

3P3V_NIA

R14 10.0K 0402
R59 8.2K 0402LF

U3
AT25128A

CS_N, SCK, SI, SO, VCC, HOLD_N, WP_N, GND

R18 8.2K 0402LF
R20 8.2K 0402LF
C43 0.1UF 0402

GND

EEPROM

EE_CS_N	C19	EE_CS_N
EE_SK	B19	EE_SK
EE_DI	B18	EE_DI
EE_DO	A18	EE_DO

R60 22 0402LF

FREQ EE_SK < 2MHZ
EE_DO HAS INTERNAL PULL UP

FLASH

FLSH_CE_N	B7	FLSH_CE_N
FLSH_SCK	A8	FLSH_SCK
FLSH_SI	B6	FLSH_SI
FLSH_SO	A7	FLSH_SO

R17 22 0402LF

FREQ FLSH_SCK = 12.5MHZ
FLSH_SO HAS INTERNAL PULL UP

SERIAL FALASH

3P3V_NIA

R15 10.0K 0402
R16 8.2K 0402LF

I12
U2
AT25F1024

CS_N, SCK, SI, SO, VCC, HOLD_N, WP_N, GND

R19 8.2K 0402LF
R21 8.2K 0402LF
C1 0.1UF 0402

GND

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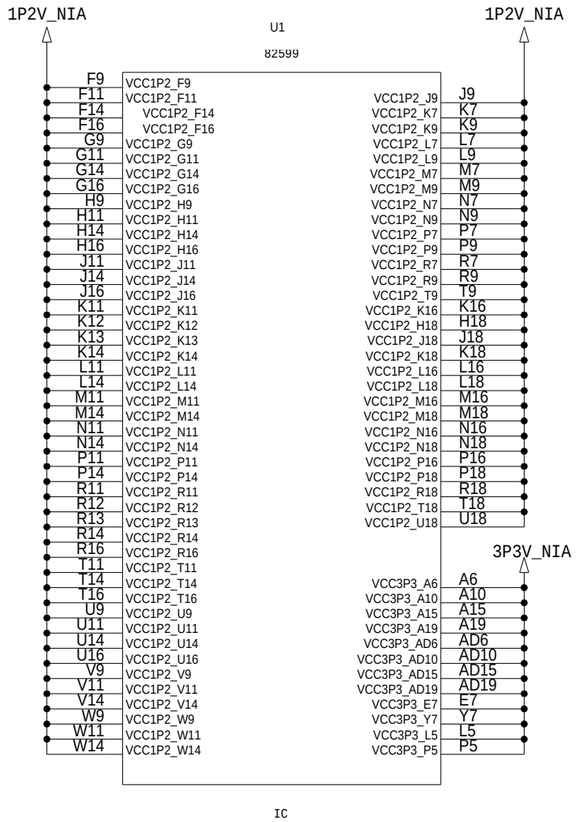
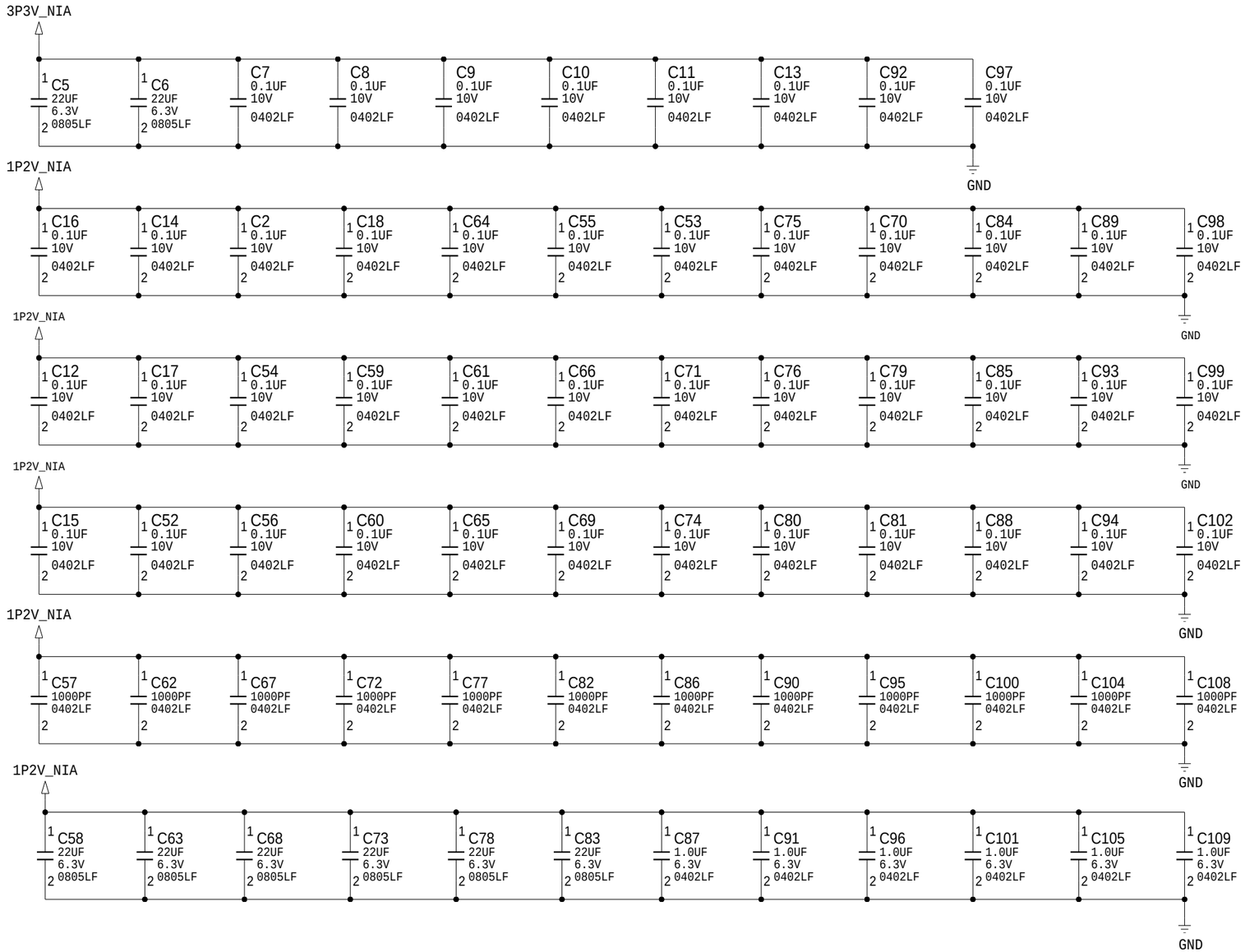
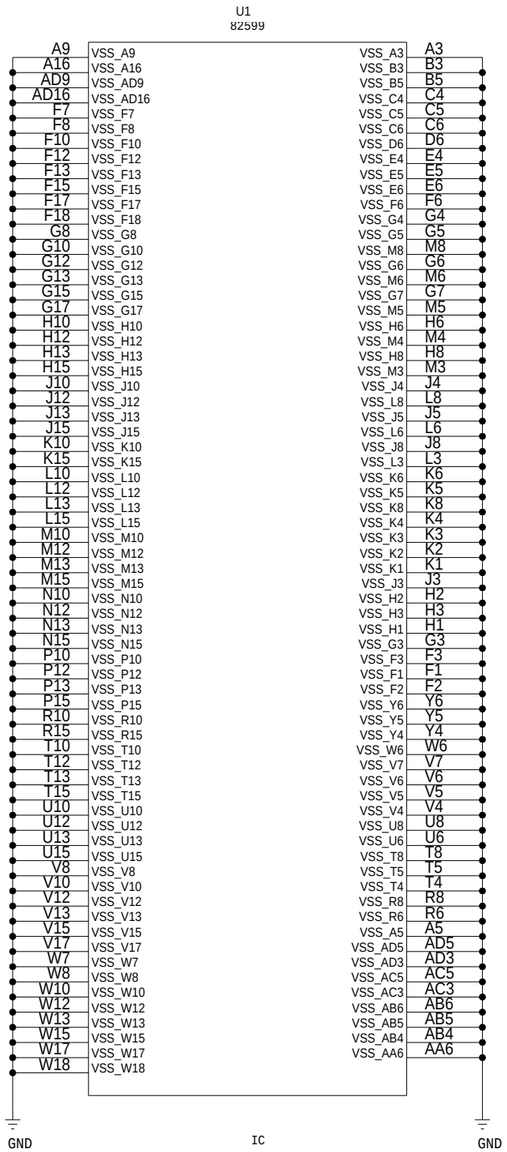
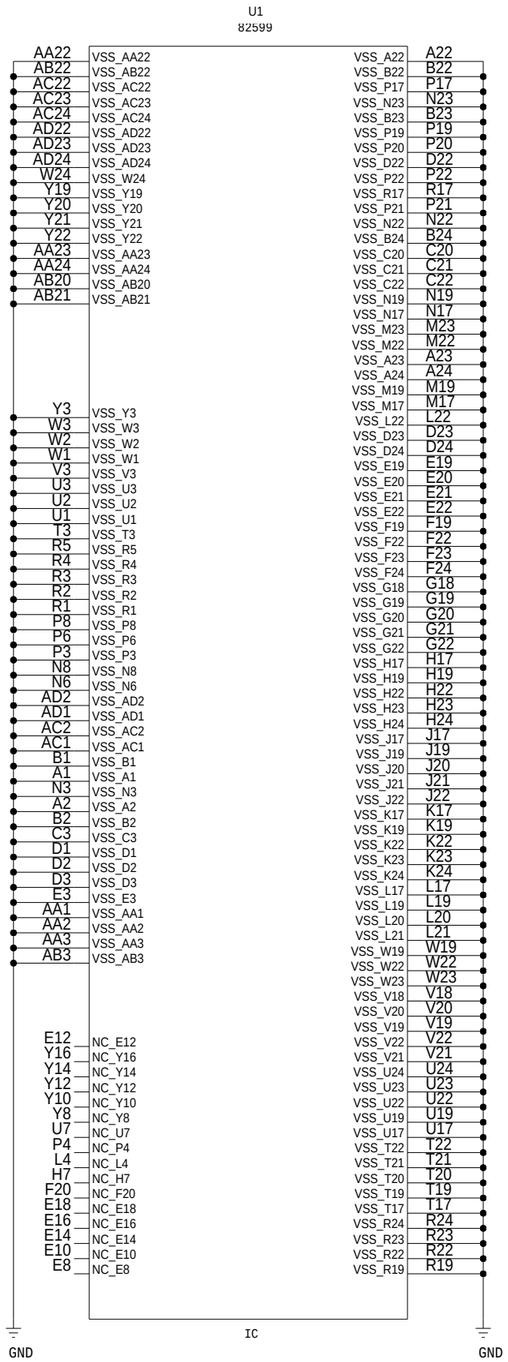




LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: 82599 - REFERENCE SCHEMATIC	SIZE: B	CODE:	DOCUMENT NUMBER:	REV: 2.3	DATE: 07/25/2012	SHEET: 7





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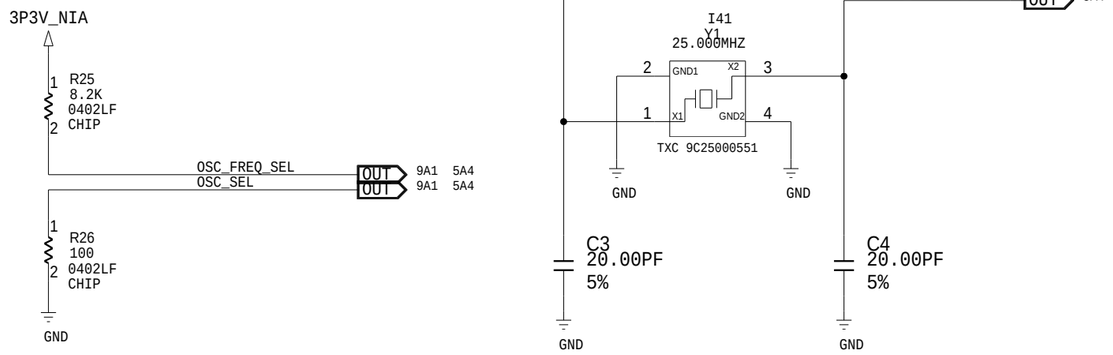
82599 REFERENCE CLOCK SOLUTION EXAMPLES

25MHZ CRYSTAL SOLUTION

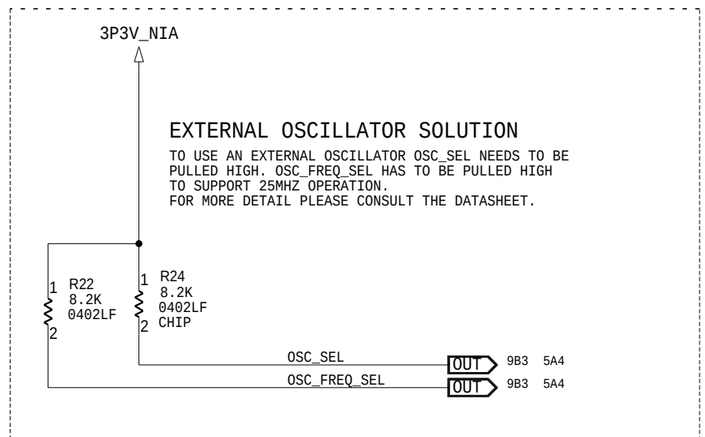
TO USE A CRYSTAL OSC_SEL NEEDS TO BE PULLED LOW, AND OSC_FREQ_SEL NEEDS TO BE PULLED HIGH TO CONFIGURE THE MULTIPLIERS CORRECTLY FOR 25MHZ CLOCK.

FOR MORE DETAIL PLEASE CONSULT THE DATASHEET.



THE 82599 ETHERNET CONTROLLER WILL ACCEPT ONE OF THE FOLLOWING TWO CLOCKING SOLUTIONS:
1) 25MHZ CRYSTAL
2) 25 MHZ DIFFERENTIAL CLOCK PROVIDED BY AN EXTERNAL OSCILLATOR.

FOR MORE DETAIL ON HOW TO CONFIGURE THE CHIP FOR ONE OF THESE THREE CLOCKING SOLUTIONS, PLEASE CONSULT THE DATASHEET.



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PORT 0: SFP+ SOLUTION

ROUTE AS 100 OHM DIFFERENTIAL PAIRS.
TRACES WITHIN A PAIR MUST BE MATCHED
WITHIN 5 MILS. PAIR TO PAIR TRACE
LENGTHS SHOULD BE MATCHED WITHIN 100 MILS

FOR MORE GUIDELINES SEE DATASHEET.

THE AC COUPLING CAPS FOR THE
SFI INTERFACE ARE INCLUDED IN
THE SFP+ MODULE

5A1 OUT RX0_L0_N
5A1 OUT RX0_L0_P

5B1 IN TX0_L0_P
5B1 IN TX0_L0_N

3.3V_SFP+_0

J3
CONN
SCONN20_SFP

11	VEER_11	VEER_10	10
12	RD-	RS1	9
13	RD+	RX_LOS	8
14	VEER_14	RS0	7
15	VCCR_15	MOD-ABS	6
16	VCCT_16	SCL	5
17	VEET_17	SDA	4
18	TD+	TX_DISABLE	3
19	TD-	TX_FAULT	2
20	VEET_20	VEET_1	1
	CHASSIS GND		
G1	CGND_1	CGND_11	G11
G2	CGND_2	CGND_12	G12
G3	CGND_3	CGND_13	G13
G4	CGND_4	CGND_14	G14
G5	CGND_5	CGND_15	G15
G6	CGND_6	CGND_16	G16
G7	CGND_7	CGND_17	G17
G8	CGND_8	CGND_18	G18
G9	CGND_9	CGND_19	G19
G10	CGND_10	CGND_20	G20

GND GND

RS0/RS1_SENSE0 BI
R28 1 2 1.50K 0402LF
RS0/RS1_DRIVE0 IN 5B3 10A2
RX_LOS0 OUT 5B3 10A2
10A2 MOD_ABS0
SCL0 IN 5B4
SDA0 BI 5B4
TX_DISABLE0 IN 5B3
TX_FAULT0 OUT 5A3 10A2

TX DISABLE HAS A 4.7-10K
PULL UP IN THE MODULE

R27 1 2 100 EMPTY 0402LF
GND

3.3V_SFP+_0
U4 IC
NC
RX_LOS0_N BI 5B3
GND
74AHC1G04
GND

3.3V_SFP+_0
U5 IC
NC
MOD_ABS0_N OUT 5B3
GND
74AHC1G04
GND

3.3V_SFP+_0
10B1 5B3 RX_LOS0 R29 1 2 10.0K 0402LF
10B2 MOD_ABS0 R65 1 2 10.0K 0402LF
10B1 5A3 TX_FAULT0 R66 1 2 10.0K 0402LF
10B1 5B3 RS0/RS1_DRIVE0 R67 1 2 1.50K 0402LF

POWER SUPPLY FILTERING

3.3V_NIA
L1 3.3UH 1 2
3P3V_SFP+_0
MAX CURRENT 750 MA
C110 0.1UF 10V 0402LF
C111 22UF 0805LF
C112 0.1UF 10V 0402LF
GND

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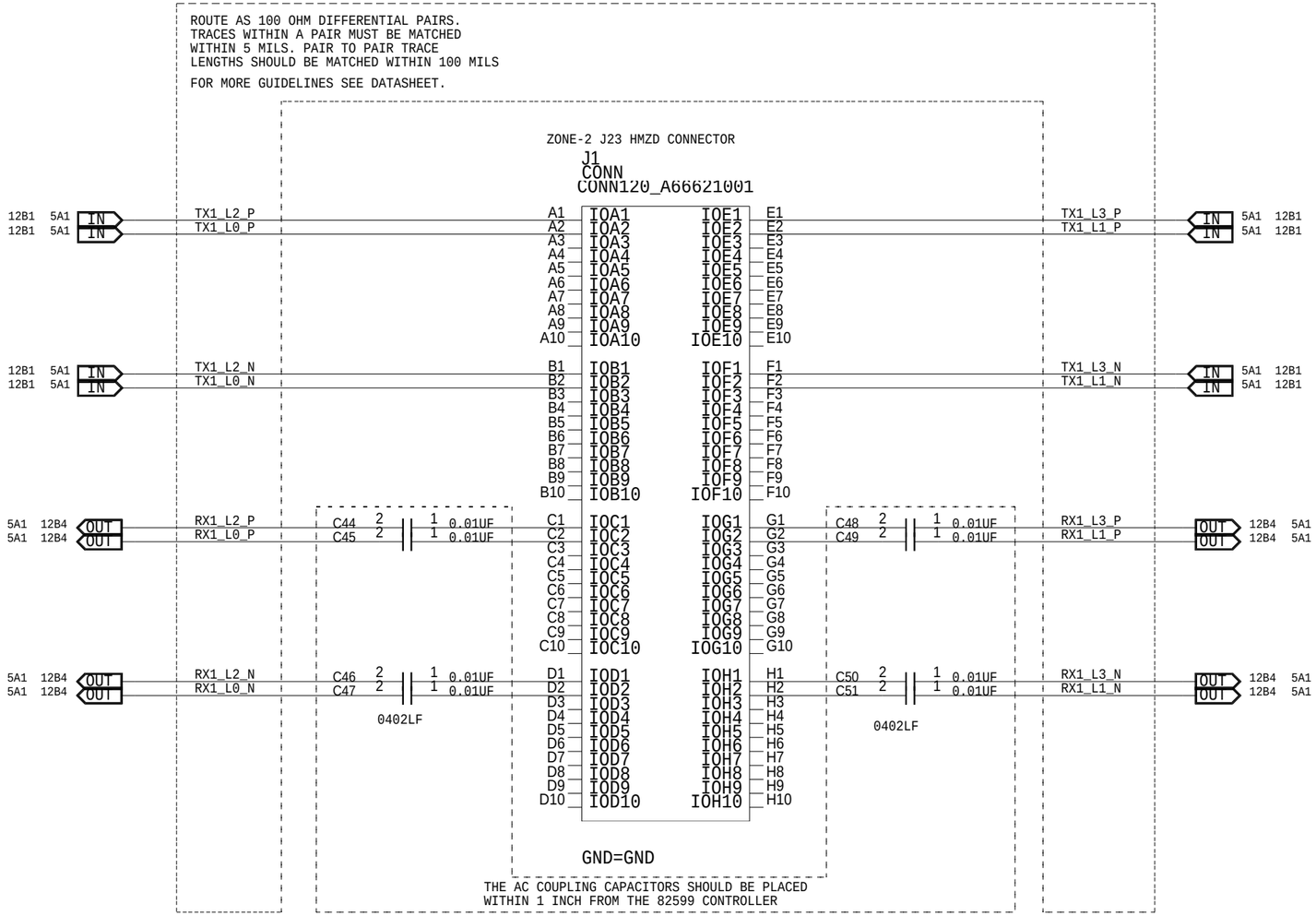
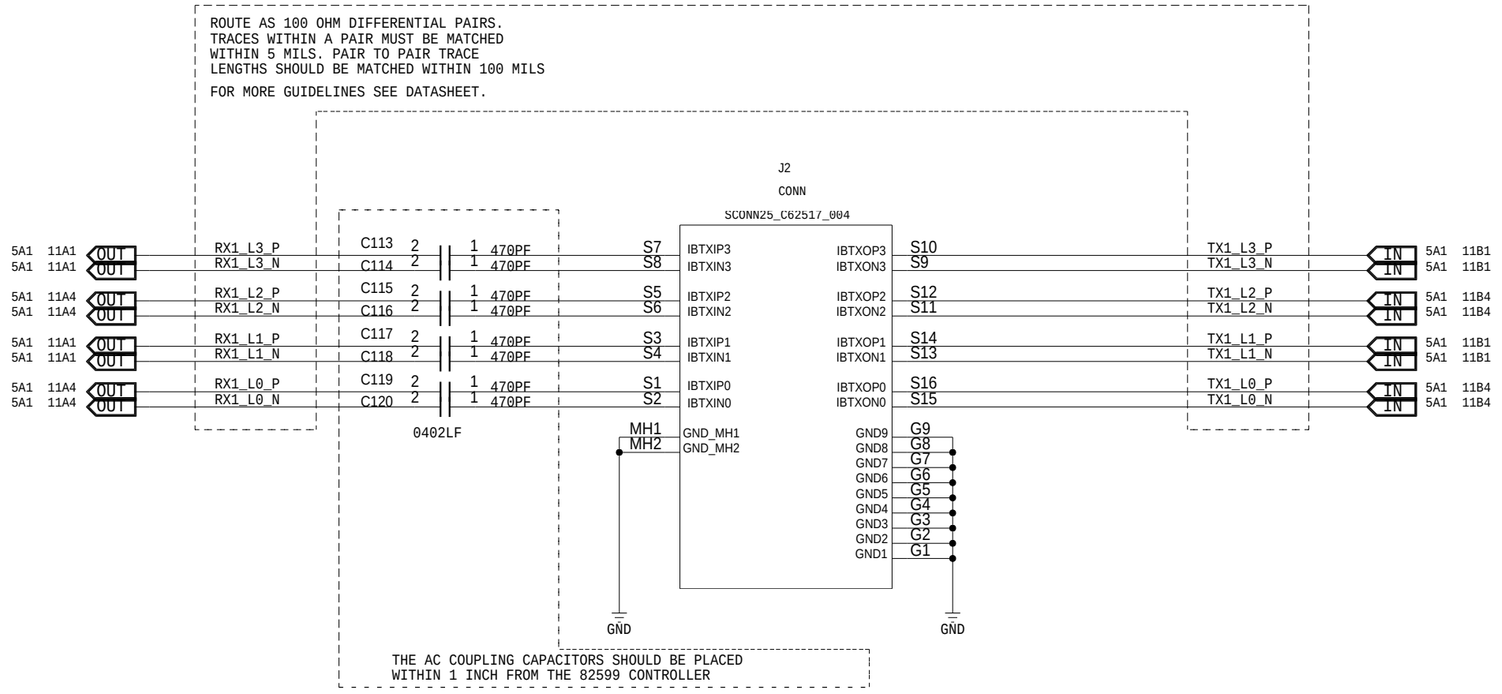
PORT 1: XAUI/KX/KX4/KR BACKPLANE SOLUTION



IF THE APPLICATION WILL USE KR SIGNALING THEN
THE LAYOUT HAS TO BE DONE WITH SPECIAL CARE.
FOR GUIDANCE PLEASE CONSULT THE DATASHEET.

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82599 - REFERENCE SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.3	DATE 07/25/2012	SHEET 11

PORT 1: CX4 SOLUTION



LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82599 - REFERENCE SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.3	DATE 07/25/2012	SHEET 12