Intel® Atom™ Processor E3800 Product Family

Thermal Design Guide

January 2016

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Revision History

Date	Revision	Description
January 2016	002	Updated SKU E3805 in Table 3 and Table 4.
October 2013	001	Initial public release.

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1.0 Introduction

Intel® Atom™ E3800 is a low power platform for intelligent systems based on the *Intel® Atom™ Processor 3800 Product Family Datasheet*. Although the thermal design power is low, the thermal solution design is still very important since typical intelligent systems can be thermally challenging due to fanless operation, mutual heating effects and relatively poor thermal interfaces.

This design guide covers package thermal performance of *Intel® Atom™ Processor 3800 Product Family Datasheet* SKUs with respect to intelligent system use conditions. Background information about thermal specifications and features can be found in the references listed in Section 1.2. The Intel Atom™ E3800 Processor Family SoC package is referred to as “SoC” in the rest of this document.

This Thermal Design Guide describes options to mechanically interface to the SoC package and the resulting thermal performance as estimated from thermal models. Future revisions of this document will include thermal performance based on test data. The SoC has been modeled as part of two small form-factor compute modules, one for print imaging applications and one for digital signage applications.

Note: This design guide does not cover the use of the SoC in automotive/IVI applications. The thermal mechanical design guide for the SoC in automotive applications will be published as a standalone document and will be available through your Intel field sales representative.

1.1 Terminology

Definitions of terms used in this document are listed in Table 1.

Table 1. Terms (Sheet 1 of 2)

Term	Definition
CFD	Computational Fluid Dynamics
ΔT_{JS}	Junction-to-heatsink temperature rise [°C]
EDS	External Design Specification
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
$\psi_{JA\text{-}MAX}$	Maximum Junction-to-ambient thermal resistance [°C/W]
ψ_{JS}	Junction-to-heatsink thermal resistance [°C/W]
ψ_{SA}	Heatsink-to-ambient thermal resistance [°C/W]
SoC	Intel Atom E3800 Processor Family System on a chip
T_{amb}	Local ambient air temperature [°C]
TDP	Thermal Design Power [W]
TIM	Thermal Interface Material
T_j	Junction temperature of component [°C]

Table 1. Terms (Sheet 2 of 2)

Term	Definition
T_{jmax}	Maximum Junction temperature rating [°C]
T_{pcb}	PCB temperature [°C]
T_{sink}	Heatsink temperature (measured above the middle of the die) [°C]

1.2 Reference Documents

The reader of this document should also be familiar with material and concepts presented in the *Intel® Atom™ Processor 3800 Product Family Datasheet*. These documents are available through your Intel field sales representative.

Table 2. Related Documents

Document	Number/Location
Intel® Atom™ Processor 3800 Product Family Datasheet	538136
Intel® Pentium® Processor N3500-series, J2850, J2900, and Intel® Celeron® Processor N2900-series, N2800-series, J1800-series, J1900, J1750 – External Design Specification (EDS)	512177
Intel® Atom™ Processor E3800 Product Family-Platform Design Guide	512379
Bay Trail-M/D Design Guide	563636
Intel® Pentium®/Celeron® J series Dual and Quad Core Processors Thermal and Mechanical Design Guide	513780
Bay Trail-M SoC Thermal Model	519627
Bay Trail-M Platform Scenario Design Power (SDP) Implementation Considerations	528014

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2.0 Specifications

2.1 Thermal Design Power

The TDP estimates for the SoC are listed in Table 3. TDP is based on running worst case real-world applications and benchmarks at maximum component temperature. TDP is not the absolute worst case power. It could, for example, be exceeded under a synthetic worst case condition or under short power spikes. The thermal solution must be designed to keep the maximum component temperature within specification while dissipating TDP.

Scenario Design Power (SDP) is a usage-based design specification, and provides additional guidance for power constrained platforms. SDP is defined at a specific scenario workload, temperature and frequency. For a detailed discussion on the definition of SDP, please refer to *Bay Trail-M Platform Scenario Design Power (SDP) Implementation Considerations* document.

Table 3. SoC Key Thermal Specifications

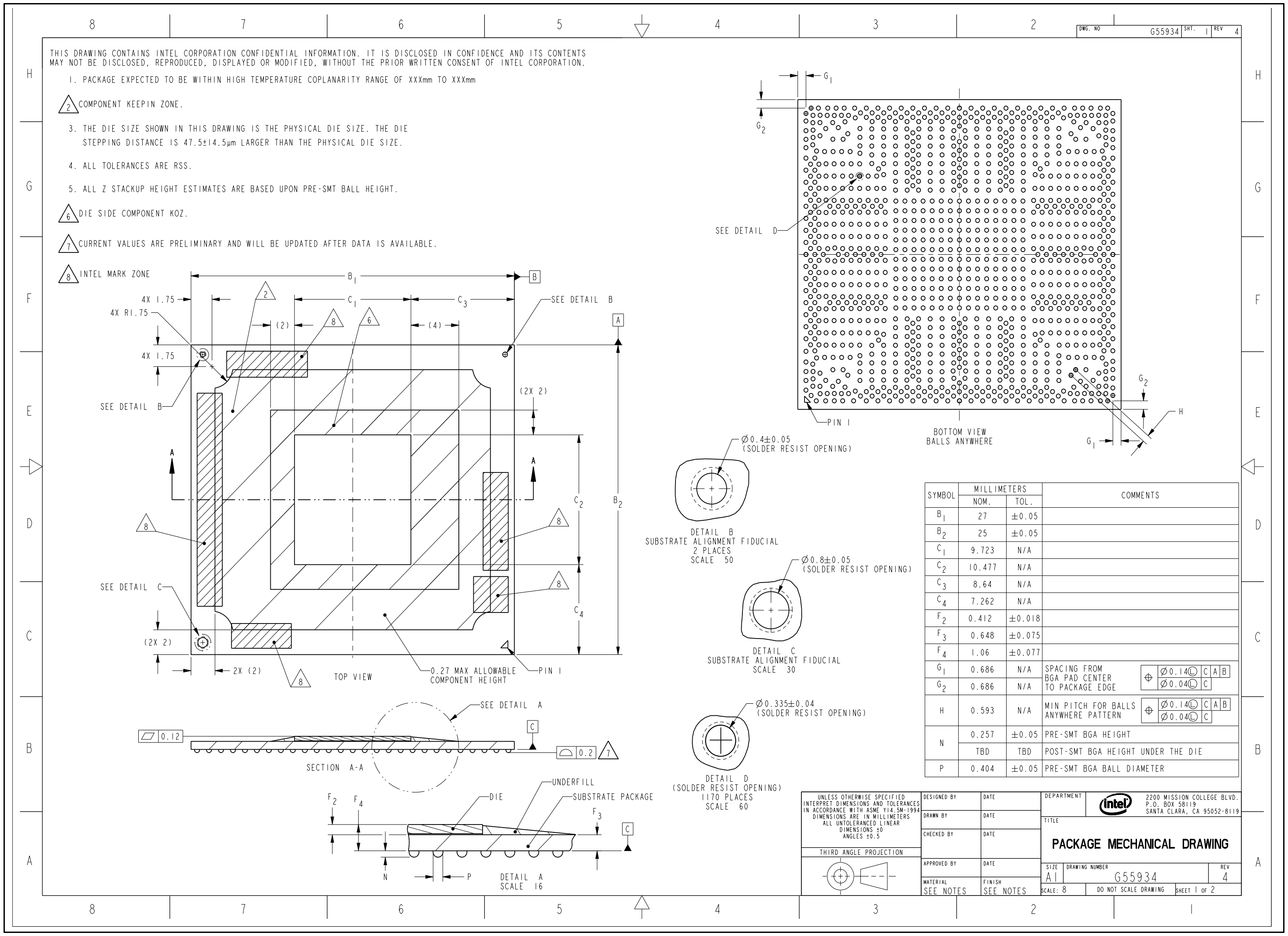
Component	TDP (SDP) W	$T_{J\text{-}MAX}$
N2910	7.5 (4.5)	100 °C
J1850	10 (N/A)	100 °C
E3805	3 (N/A)	110 °C
E3815	5 (N/A)	110 °C
E3825	6 (N/A)	110 °C
E3826	7 (N/A)	110 °C
E3827	8 (N/A)	110 °C
E3845	10 (N/A)	110 °C

2.2 Packaging Information

The SoC utilizes a 25 x 27 mm FCBGA package as shown in Figure 1. The FCBGA package is a bare die package and will be in direct contact with the thermal solution. Note that there are capacitors near the die. Although the die-side capacitors are slightly shorter than the silicon die, be careful to avoid contacting the capacitors with electrically conductive materials or a heatsink base. Consider using an insulating material between the capacitors and heatsink to prevent capacitor shorting.

The data provided in this section is for reference purposes only. Refer to the device's most recent *External Design Specification* (EDS) for up-to-date information. In the event of conflict, the device's EDS supersedes data shown in these figures.

Figure 1. Mechanical Drawing



THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

1. PACKAGE EXPECTED TO BE WITHIN HIGH TEMPERATURE COPLANARITY RANGE OF XXXmm TO XXXmm
2. COMPONENT KEEPIN ZONE.
3. THE DIE SIZE SHOWN IN THIS DRAWING IS THE PHYSICAL DIE SIZE. THE DIE STEPPING DISTANCE IS 47.5±14.5µm LARGER THAN THE PHYSICAL DIE SIZE.
4. ALL TOLERANCES ARE RSS.
5. ALL Z STACKUP HEIGHT ESTIMATES ARE BASED UPON PRE-SMT BALL HEIGHT.
6. DIE SIDE COMPONENT KOZ.
7. CURRENT VALUES ARE PRELIMINARY AND WILL BE UPDATED AFTER DATA IS AVAILABLE.
8. INTEL MARK ZONE

SYMBOL	MILLIMETERS		COMMENTS	
	NOM.	TOL.		
B_1	27	±0.05		
B_2	25	±0.05		
C_1	9.723	N/A		
C_2	10.477	N/A		
C_3	8.64	N/A		
C_4	7.262	N/A		
F_2	0.412	±0.018		
F_3	0.648	±0.075		
F_4	1.06	±0.077		
G_1	0.686	N/A	SPACING FROM BGA PAD CENTER TO PACKAGE EDGE	⌖ Ø0.14Ⓛ C A B Ø0.04Ⓛ C
G_2	0.686	N/A		
H	0.593	N/A	MIN PITCH FOR BALLS ANYWHERE PATTERN	⌖ Ø0.14Ⓛ C A B Ø0.04Ⓛ C
N	0.257	±0.05	PRE-SMT BGA HEIGHT	
	TBD	TBD	POST-SMT BGA HEIGHT UNDER THE DIE	
P	0.404	±0.05	PRE-SMT BGA BALL DIAMETER	

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3.0 Thermal Solution Design

3.1 Thermal Solution Characterization

The thermal characterization parameter ψ ("psi"), is used to characterize thermal solution performance, as well as compare thermal solutions in identical situations (i.e., heating source, local ambient conditions, etc.). It is defined by the following equation.

Equation 1. Junction-to-Local Ambient Thermal Characterization Parameter (ψ_{JA})

$$\Psi_{JA} = \frac{T_{J-MAX} - T_{LA}}{TDP}$$

where,

ψ_{JA} = Junction-to-local ambient thermal characterization parameter (°C/W)

$T_{J\text{-}MAX}$ = Maximum allowed device temperature (°C)

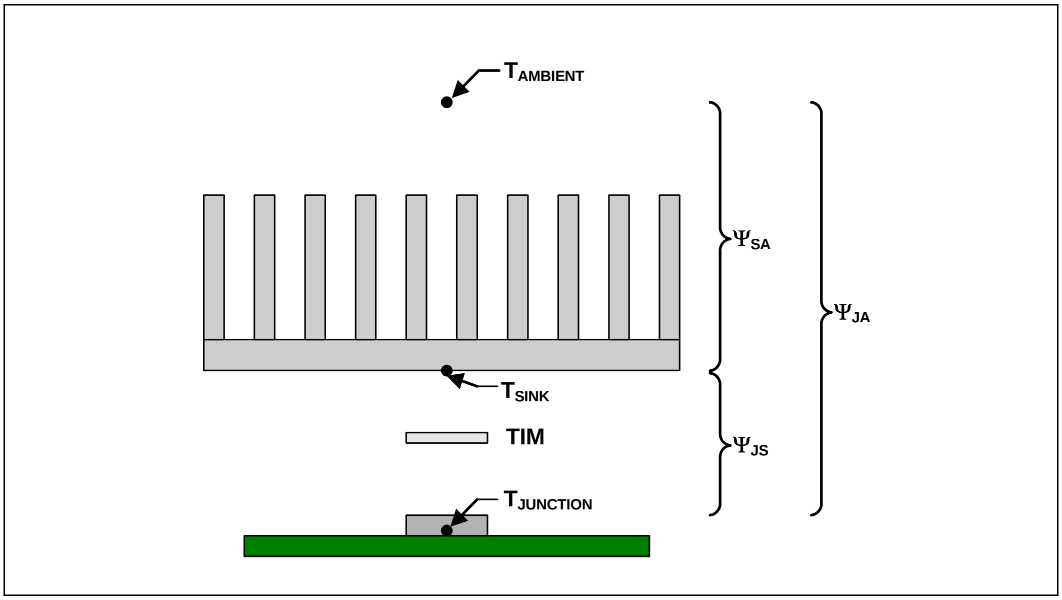
T_{LA} = Local ambient temperature near the device (°C)

TDP = Thermal Design Power (W) at the package level

The thermal characterization parameter assumes that all package power dissipation is through the thermal solution (heatsink), and is equal to TDP. A small percentage of the die power (< 5%) is dissipated through the package/motherboard stack to the environment, and should not be considered as a means of thermal control.

The temperatures of interest are shown in Figure 2. These temperatures are measurable temperatures as needed for design verification. The processor $T_{JUNCTION}$ is readable by on-die sensors, while all other temperatures can be measured with thermocouples.

Figure 2. Model Temperatures



The primary heat transfer path for the SoC is shown in Equation 2 as a thermal resistor network.

Equation 2. Thermal Resistance

$$\Psi_{JA} = \Psi_{JS} + \Psi_{SA}$$

Where:

ψ_{JS} = Thermal characterization parameter from junction-to-sink, this also includes thermal resistance of the thermal interface material (ψ_{TIM}) (°C/W).

ψ_{SA} = Thermal characterization parameter from sink-to-local ambient (°C/W)

The junction-to-local ambient thermal characterization parameter, ψ_{JA}, is composed of ψ_{JS}, which includes the thermal interface material thermal characterization parameter, and of ψ_{SA}, the sink-to-local ambient thermal characterization parameter. ψ_{SA} is a measure of the thermal characterization parameter from the bottom of the heatsink to the local ambient air. ψ_{SA} is dependent on the heatsink material, thermal conductivity, and geometry. It is also strongly dependent on the air velocity through the fins of the heatsink.

3.2 Thermal Performance Requirements

Overall thermal performance, ψ_{JA}, is then defined using the thermal characterization parameter:

- Define a target component temperature $T_{JUNCTION}$ and corresponding TDP.
- Define a target local ambient temperature, T_{LA}.

The following provides an illustration of how to determine the appropriate performance targets.

Assume:

- TDP = 10 W and $T_{JUNCTION}$ = 100 °C
- Local processor ambient temperature, T_A = 55 °C

Using Equation 1 the maximum allowable resistance, junction-to-ambient, is calculated as:

Equation 3. Maximum Allowable Resistance Calculation

$$\psi_{JA} = \frac{T_{J-MAX} - T_{LA}}{TDP} = \frac{100 - 55}{10} = 4.5\,°C/W$$

To determine the required heatsink performance, a heatsink solution provider would need to determine ψ_{JA} performance for the selected TIM and mechanical load configuration. If the heatsink solution were designed to work with a TIM material performing at $\psi_{JS} \leq 0.3$ °C/W, solving from Equation 2, the performance of the heatsink required is shown in Equation 4.

Equation 4. Required Heatsink Performance

$$\psi_{SA} = \psi_{JA} - \psi_{JS} = 4.5 - 0.3 = 4.2\,°C/W$$

It is evident from the above calculations that a reduction in the local ambient temperature can have a significant effect on the junction-to-ambient thermal resistance requirement. This effect can contribute to a more reasonable thermal solution including reduced cost, heatsink size, heatsink weight, or a lower system airflow rate. The required heatsink performance for all the SKUs at local ambient conditions of 45 °C, 55 °C and 65 °C are shown in Table 4 below.

Table 4. *Intel® Atom™ Processor 3800 Product Family Datasheet* Thermal Design Requirements

Component	TDP (W)	ψ_{JS}	ΔT_{JS} (°C)	Allowable T_{sink} (°C)	ψ_{SA}(°C/W)		
					T_{amb} = 45 °C	T_{amb} = 55 °C	T_{amb} =65 °C
N2910	7.5	0.3	2.25	97.75	7.0	5.7	4.4
J1850	10	0.3	3	97	5.2	4.2	3.2
E3805	3	0.3	0.9	109.1	21.4	18	14.7
E3815	5	0.3	1.5	108.5	12.7	10.7	8.7
E3825	6	0.3	1.8	108.2	10.5	8.9	7.2
E3826	7	0.3	2.1	107.9	9	7.6	6.1
E3827	8	0.3	2.4	107.6	7.8	6.6	5.3
E3845	10	0.3	3	107	6.2	5.2	4.2

The numbers shown in the table above are thermal guidance numbers for a given T_{LA} and a given TIM performance (0.3 °C/W). These numbers will change based on the TIM used, the mechanical retention mechanism and the actual T_{LA} in the design. Two scenarios have been modeled to understand how these numbers vary with design.

3.3 System Models

To investigate SoC thermal performance within an intelligent system, computational fluid dynamic models were created for digital signage and print imaging form factors. The PCB for both these models contain the SoC, a PMIC, a LAN controller, memory and other heat dissipating components.

For the digital signage model a thermal solution is modeled that uses the chassis to sink the heat from the SoC, the LAN controller and the PMIC, as shown in Figure 3. The chassis top is employed to sink the heat and is shown as a finned heatsink. For the print imaging applications model, a component heat sink is used for cooling the SoC with a system fan cooling the chassis as shown in Figure 4.

These are example configurations to investigate interface conditions and the resulting thermal performance of the SoC. Other configurations are possible, but from a thermal performance perspective these configurations will give a good indication of basic SoC thermal performance.

Figure 3. Digital Signage Model

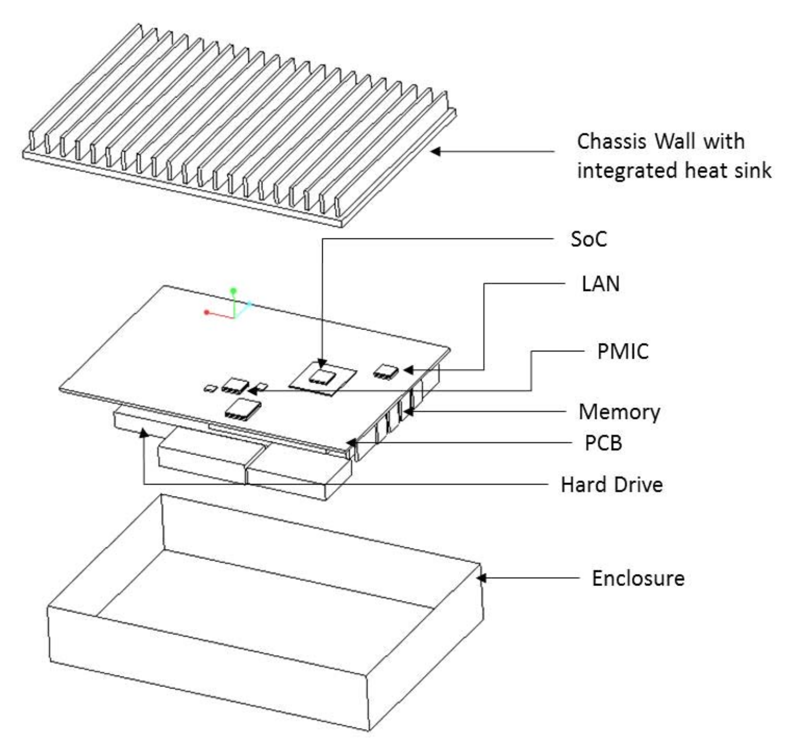
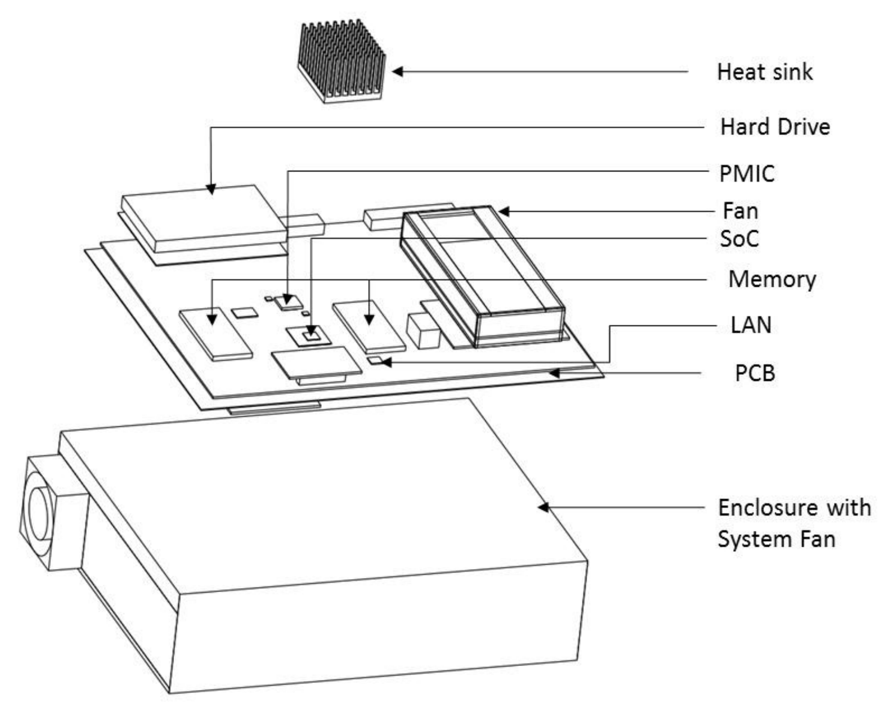


Figure 4. Print Imaging Model



3.4 Heat Sink Interface

The mechanical interface between the chassis based heatsink and the components (SoC, LAN controller and PMIC) in the digital signage model is complicated by the different component heights and tolerances. To account for the height deltas and tolerance differences between the components, use gap pads and/or thick phase-change materials, depending on the mounting reference of the heat spreader assembly.

For print imaging applications, a component heatsink is used for the SoC; you can use phase-change material as the thermal interface material.

3.5 System Thermal Model Parameters and Assumptions

The system model was created using Computational Fluid Dynamics (CFD) modeling software called Icepak* and FloTHERM* to determine the key temperatures for the two form factors noted above. Table 5 lists some of the modeling parameters for the two form factors.

Table 5. Modeling Parameters

Parameter	Digital Signage Form Factor		Print Imaging Form Factor	
TIM properties	Gap Pad Conductivity: 6 W/mK		Phase Change Material Thermal Impedance: 0.2 °C-cm^2/W	
Thermal solution	Aluminum (Al-2024-T6) chassis based solution with copper pedestals		Aluminum Heatsink (Al-2024-T6)	
SoC TDP	7.5W T_{jmax}: 100 °C (N2910)	10 W T_{jmax}:100 °C (J1850)	5 W T_{jmax}: 110 °C (E3810)	10W T_{jmax}: 110 °C (E3840
LAN controller power	0.4 W		0.4 W	
PMIC power	2.3 W		2.3 W	
Memory power	8 x 400 mW (3.2 W)		8 x 400 mW (3.2 W)	
Hard drive	5 W		5 W	
System fan	Not Applicable		15.5 CFM (Fan power=0.96 W)	
System power	23.4 W	25.9 W	37.15 W	42.15 W

3.6 Digital Signage Thermal Modeling Results

The CFD model was run for the digital signage form factor to determine the processor junction temperature with a heatsink integrated with the chassis cooling the SoC, LAN controller and the PMIC.

The following results for the analysis are based on the following constants:

- SoC: T_{jmax}: 100 °C

And the following calculations were made:

- Junction-to-heatsink temperature rise: ΔT_{JS} = TDP x ψ_{JS}
- Allowable heatsink temperature: $T_{sink} = T_{jmax} - \Delta T_{JS}$
- Heatsink resistance: $\psi_{SA} = (T_{sink} - T_{amb})$ / TDP

Table 7 gives three different ψ_{SA} values based on three different ambient temperatures: 35 °C, 45 °C and 55 °C and these results are based on the use of the chassis wall with an integrated heatsink as a thermal solution. The chassis top is modeled as a finned 184 mm x 125 mm x 15 mm aluminum heat sink with 21 fins (2 mm thick) and uses pedestals for interfacing to the SoC, the LAN controller and the PMIC. The magnitude of the ψ_{SA} values gives an indication of the type of thermal solution required.

Table 6. Digital Signage Thermal Model Tabular Results

Component	TDP (W)	ψ_{JS}	ΔT_{JS} (°C)	Allowable T_{sink}(°C)	ψ_{SA}(°C/W)		
					T_{amb} = 35 °C	T_{amb} = 45 °C	T_{amb} =55 °C
N2910	7.5	1.9	14.25	85.75	6.8	5.4	4.1
J1850	10	1.9	19	81	4.6	3.6	2.6

For the digital signage form factor, with the use of a Gap Pad material as TIM up to the ambient condition of 45 °C, the required ψ_{SA} matches up to typical heatsinks for fanless designs.

3.7 Print Imaging Thermal Modeling Results

The CFD model was run for the print imaging form factor option to determine the processor junction temperature with a basic component heatsink for the SoC in a chassis with system airflow.

The following results for the three options are based on the following constants:

- SoC: T_{jmax}: 110 °C

And the following calculations were made:

- Junction-to-heatsink temperature rise: $\Delta T_{JS} = TDP \times \psi_{JS}$
- Allowable heatsink temperature: $T_{sink} = T_{jmax} - \Delta T_{JS}$
- Heatsink resistance: $\psi_{SA} = (T_{sink} - T_{amb}) / TDP$

Table 7 gives three different ψ_{SA} values based on three different ambient temperatures: 35 °C, 45 °C and 55 °C. The component heatsink employed in the print imaging CFD model is a 55 mm x 55 mm x 35 mm finned aluminum heat sink with 1.5 mm thick pins. The magnitude of the ψ_{SA} values gives an indication of the type of thermal solution required.

Table 7. Print Imaging Thermal Model Tabular Results

Component	TDP (W)	ψ_{JS}	ΔT_{JS} (°C)	Allowable T_{sink}(°C)	ψ_{SA}(°C/W)		
					T_{amb} = 35 °C	T_{amb} = 45 °C	T_{amb} =55 °C
E3815	5	0.3	1.5	108.5	14.7	12.7	8.7
E3825	6	0.3	1.8	108.2	12.2	10.5	8.9
E3826	7	0.3	2.1	107.9	10.4	9	7.6
E3827	8	0.3	2.4	107.6	9	7.8	6.6
E3845	10	0.3	3	107	7.2	6.2	5.2

For the print imaging form factor, with the use of a phase-change material as TIM and system airflow, up to the ambient condition of 55 °C, the required ψ_{SA} matches up to typical aluminum heatsinks.

3.8 Thermal Modeling Tools and Resources

The SoC system models are based on digital signage and print imaging applications. The thermal performance results are dependent on the boundary conditions stipulated in the model. For all applications, customers are encouraged to use the package model as part of their overall system model. The package model will be 3D model available for Icepak* and Flotherm* thermal analysis tools.

Intel also provides thermal consultation for questions about this document and the application of the SoC in customer-specific applications. For both models and consultation help, please contact your Field Application Engineer.

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