Intel® Celeron® Processor J1800, J1900, N2807, and N2930 for Internet of Things

Specification Update Addendum

June 2018
## Contents

1.0 Preface ........................................................................................................................................... 5
  1.1 Affected Documents ................................................................................................................. 5  
  1.2 Related Documents .................................................................................................................. 5  
  1.3 Nomenclature .......................................................................................................................... 5 

2.0 Summary Tables of Changes ........................................................................................................ 7
  2.1 Codes Used in Summary Table .................................................................................................. 7  
  2.2 Stepping .................................................................................................................................... 7  
  2.3 Status ......................................................................................................................................... 7  
  2.4 Row ........................................................................................................................................... 7 

3.0 Errata Summary ............................................................................................................................... 8
  3.1 SPECIFICATION CHANGES .................................................................................................................. 8  
  3.2 SPECIFICATION CLARIFICATIONS ................................................................................................. 8  
  3.3 DOCUMENTATION CHANGES ........................................................................................................ 8 

4.0 Identification Information .............................................................................................................. 9
  4.1 Component Identification via Programming Interface ............................................................... 9  
  4.2 Component Marking Information ................................................................................................ 9 

5.0 Errata .......................................................................................................................................... 11
  5.1 VLPI1. System May Experience Inability to Boot or May Cease Operation................................. 11  
  5.2 VLPI2. Reset Sequence may Not Complete Under Certain Conditions .................................... 11 

6.0 Specification Changes .................................................................................................................... 12 

7.0 Specification Clarifications ........................................................................................................... 13 

8.0 Documentation Changes .............................................................................................................. 14 

**Revision History**

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2018</td>
<td>002</td>
<td>Updated to include Intel® Celeron® J1800 Processor and VLPI2 information</td>
</tr>
<tr>
<td>July 2017</td>
<td>001</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
1.0 Preface

This document is an update to the specifications in the following Affected Documents and Related Documents tables. It is a compilation of device and document errata, and specification clarifications and changes. This document is intended for hardware system manufacturers and software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

**Note:** This document is a supplement to the Intel® Celeron® and Pentium® Processor N – and J – Series Specification Update. The document contains specification updates unique to the implementation and operation of the Intel® Celeron® processors J1800, J1900, N2807, and N2930 in Internet of Things platforms.

1.1 Affected Documents

<table>
<thead>
<tr>
<th>Document Title</th>
<th>Document Number/Location</th>
</tr>
</thead>
</table>

1.2 Related Documents

<table>
<thead>
<tr>
<th>Document Title</th>
<th>Document Number/Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Celeron® and Pentium® Processor N – and J – Series Specification Update</td>
<td>329671</td>
</tr>
</tbody>
</table>

1.3 Nomenclature

**Errata** are design defects or errors. Errata may cause the processor’s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

**Note:** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).
## 2.0 Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### 2.1 Codes Used in Summary Table

### 2.2 Stepping

**X:** Erratum, Specification Change or Clarification that applies to this stepping.

(No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to list stepping.

### 2.3 Status

**Doc:** Document change or update that will be implemented.

**Plan Fix:** This erratum may be fixed in a future stepping of the product.

**Fixed:** This erratum has been previously fixed.

**No Fix:** There are no plans to fix this erratum.

### 2.4 Row

| Shaded: | This item is either new or modified from the previous version of the document. |
3.0  Errata Summary

Table 1. Errata Summary

<table>
<thead>
<tr>
<th>Number</th>
<th>Status</th>
<th>Steppings</th>
<th>ERRATA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>B2</td>
<td>B3</td>
</tr>
<tr>
<td>VLPI11</td>
<td>Fixed</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>VLPI2</td>
<td>Fixed</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

NOTE:
1. This erratum is not relevant to Intel® Celeron® Processor J1800 since it is not supported for use in embedded use conditions

3.1  SPECIFICATION CHANGES

<table>
<thead>
<tr>
<th>Number</th>
<th>SPECIFICATION CHANGES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>There are no Specification Changes in this Specification Update revision.</td>
</tr>
</tbody>
</table>

3.2  SPECIFICATION CLARIFICATIONS

<table>
<thead>
<tr>
<th>Number</th>
<th>SPECIFICATION CLARIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>There are no Specification Clarifications in this Specification Update revision.</td>
</tr>
</tbody>
</table>

3.3  DOCUMENTATION CHANGES

<table>
<thead>
<tr>
<th>Number</th>
<th>DOCUMENTATION CHANGES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>There are no Documentation Changes in this Specification Update revision.</td>
</tr>
</tbody>
</table>
4.0 Identification Information

4.1 Component Identification via Programming Interface

The Intel® Celeron® processor J1800, J1900, N2807, and N2930 stepping can be identified by the following register contents:

Table 2. Component Identification via Programming Interface

<table>
<thead>
<tr>
<th>Reserved</th>
<th>Extended Family</th>
<th>Extended Model</th>
<th>Reserved</th>
<th>Processor Type</th>
<th>Family Code</th>
<th>Model Number</th>
<th>Stepping ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000b</td>
<td>0000000b</td>
<td>0011b</td>
<td>000b</td>
<td>0b</td>
<td>0110b</td>
<td>0111b</td>
<td>B3: 0011b C0: 0100b D1:1001b</td>
</tr>
</tbody>
</table>

NOTES:
1. The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® Pro, Pentium® 4, or Intel® Core™ processor family.
2. The Extended Model, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Processor Type, specified in bits [13:12] indicates whether the processor is an original OEM processor, an OverDrive processor, or a dual processor (capable of being used in a dual processor system).
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with 1 in the EAX register, and the model field of the Device ID register, accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. See Table 3 for the processor stepping ID number in the CPUID information.

When EAX is initialized to a value of 1, the CPUID instruction returns the Extended Family, Extended Model, Type, Family, Model, and Stepping value in the EAX register.

Note: The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

4.2 Component Marking Information

The Intel® Celeron® processor J1800, J1900, N2807, and N2930 are identified by the following component markings:
Sample Marking Information:

**GRP1LINE1:** i{M}{C}YY_FPO12345
**GRP2LINE1:** QDF / SSPEC
**GRP3LINE1:** {e1}

Table 3. Identification Table for Intel® Celeron® Processor J1800, J1900, N2807, and N2930

<table>
<thead>
<tr>
<th>QDF / S-Spec</th>
<th>MM#</th>
<th>Product Stepping</th>
<th>Processor #</th>
<th>CPUID</th>
<th>Core Speed</th>
<th>Package</th>
<th>Cache Size (KB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Highest Freq. Mode (HFM)/ Burst GHz</td>
<td>Lowest Freq. Mode (LFM) MHz</td>
<td></td>
</tr>
<tr>
<td>SR1SC</td>
<td>932481</td>
<td>B3</td>
<td>J1900</td>
<td>30673</td>
<td>2.00/2.42 (B)</td>
<td>1333</td>
<td>Micro-FCBGA13</td>
</tr>
<tr>
<td>SR1UT</td>
<td>934010</td>
<td>C0</td>
<td>J1900</td>
<td>30678</td>
<td>2.00/2.42 (B)</td>
<td>1333</td>
<td>Micro-FCBGA13</td>
</tr>
<tr>
<td>SR1W3</td>
<td>934896</td>
<td>C0</td>
<td>N2930</td>
<td>30678</td>
<td>1.83/2.17 (B)</td>
<td>1333</td>
<td>Micro-FCBGA13</td>
</tr>
<tr>
<td>SR1W5</td>
<td>934898</td>
<td>C0</td>
<td>N2807</td>
<td>30678</td>
<td>1.58/2.17 (B)</td>
<td>1333</td>
<td>Micro-FCBGA13</td>
</tr>
</tbody>
</table>

**NOTE:** 'B' is the Intel® Burst Technology x.x (x.x is a placeholder for future versions) feature that is included in the Refresh SKU.
5.0 Errata

5.1 VLPI1. System May Experience Inability to Boot or May Cease Operation

Problem: Under certain conditions where activity is high for several years the LPC, USB (low speed and full speed) and SD Card circuitry may stop functioning in the outer years of use.

Implication: LPC circuitry that stops functioning may cause operation to cease or inability to boot. SD Card or USB circuitry that stops functioning may cause SD Cards to be unrecognized or Low Speed or Full Speed USB devices to not function. Intel has only observed this behavior in simulation. Designs that implement the LPC interface at the 1.8V signal voltage are not affected by the LPC part of this erratum.

Workaround: Firmware code changes for LPC circuitry and mitigations for SD Card & USB circuitry have been identified and may be implemented for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

5.2 VLPI2. Reset Sequence may Not Complete Under Certain Conditions

Problem: Under certain conditions, the SoC may not complete initialization either during a reset issued while the system is running, or from the G3 (mechanical off) global system state.

Implication: When this erratum occurs, the SoC will detect an initialization problem and halt the initialization sequence prior to normal operation, leading to a system hang. The system will subsequently require a power cycle via the system power button.

Workaround: For the erratum occurring during reset, while the system is running, a firmware code change has been identified. This change significantly reduces the likelihood of this initialization erratum after initial reset, at power on.

In the rare situation of this sighting occurring, the end user is expected to execute a global reset by performing a Power Button Override (press and hold the power button for approximately 4 seconds).

Status: For the steppings affected, see the Summary Tables of Changes.
6.0 Specification Changes

There are no Specification Changes in this Specification Update revision.
7.0 Specification Clarifications

There are no specification clarifications in this Specification Update revision.
8.0  Documentation Changes

The following register is an addition to section 32.12 of the Datasheet that implements an incremental method for software to differentiate between processor steppings.

**Manufacturer ID (PCIE_REG_MANUFACTURER_ID) - Offset F8h**

**Access Method**

**Type:** PCI Configuration Register  
**PCIE_REG_MANUFACTURER_ID:** [B:0, D:31, F:0] + F8h  
(Size 32 bits)

**Default:** 01xx0F1Ah

<table>
<thead>
<tr>
<th>Bit Range</th>
<th>Default &amp; Access</th>
<th>Field Name (ID): Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>01h RO</td>
<td>RSVD0: Reserved</td>
</tr>
</tbody>
</table>
| 23:16     | xxh RO           | Manufacturing Stepping ID (MSID): This value of this field depends on the stepping of the processor  
|           |                  | — B2: 0Ah                    |
|           |                  | — B3: 0Ch                    |
|           |                  | — C0: 0Eh                    |
|           |                  | — D1: 13h                    |
| 15:0      | 0F1Ah RO         | RSVD1: Reserved              |