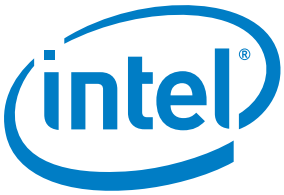

Intel® Core™ i5-3610ME Processor (PGA) and Mobile Intel® QM77 Express Chipset Development Kit

User Guide

November 2012

Document Number: 328076-001

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Revision History

Date	Revision	Description
November 2012	1.0	Initial release.

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1 Introduction

This User Guide describes the typical hardware set-up procedures, features, and use of the Intel® Core™ i5-3610ME Processor (PGA) and Mobile Intel® QM77 Express Chipset Development Kit. Read this document in its entirety prior to powering ON. The Quick Start document provides quick start procedures for reference. It is recommended to have the schematics present as you proceed through this document.

The Intel® Core™ i5-3610ME Processor (PGA) and Mobile Intel® QM77 Express Chipset Development Kit is a dual channel DDR3 mobility platform. It is designed to support the Ivy Bridge and Sandy Bridge processors and the Panther Point-M Chipset.

1.1 Terminology

Table 1. Terminology

Term	Description
ACPI	Advanced Configuration + Power Interface
AHCI	Advanced Host Controller Interface for Serial ATA
BCLK	FSB Clock used for CPU Clock domain (Eg: 167/200/266/333)
BIOS	Basic Input Output System
CMOS	Refers to the non-volatile configuration memory in the PCH
DDR3	Double Data Rate Synchronous Dynamic Random Access Memory third generation
DP	Display Port
DVI	Digital Visual Interface
eDP	Embedded Display Port
GND	Signal Ground
HDD	Hard disk drive
HDMI	High Definition Multimedia Interface
HSD	High Speed Database
IMVP-6	Intel Mobile Voltage Positioning 6
ITP-XDP	In-target-probe – eXtended debug port

Term	Description
JTAG	Joint Test Action Group, IEEE 1149.1 standard for test access port and boundary scan.
LVDS	Low-voltage Differential Signaling
OS	Operating System
PCH	Platform Controller Hub
PCI	Peripheral Component Interface
PCIe	Peripheral Component Interface Express
POST	Power-On Self Test
PPT	Panther Point
PS2	Programming System 2 (IBM) defines keyboard and mouse interface
S3	"Save to RAM" Sleep State
S5	"Soft Off" Sleep State
SATA	Serial - Advanced Technology Attachment
SIO	Super Input Output device
SLP	Sleep
SMBUS	System Management Bus, a two wire serial bus used for low-bandwidth communication
SO-DIMM	Memory Module
USB	Universal Serial Bus
VAC	Volt AC
VCC	Used to signify circuit logic voltage
VDC	Volt DC
VDD	Used to signify DIMM logic supply voltage
VGA	Video Graphics Array
VID	Voltage Identification
VREF	Voltage reference
VSS	Used to signify ground connection
VTT	Used to signify signal termination voltage

Term	Description
VTT	Voltage Transient Test tool
XDP	eXtended Debug Port (See ITP-XDP)

1.2 Reference Documents

Table 2. Reference Documents

Document	Document No./Location
Intel® Core™ i5-3610ME Processor (PGA) and Mobile Intel® QM77 Express Chipset Development Kit Quick Start Guide	328077

1.3 Development Kit Items

The development kits include these items.

Note: All kit items need to be specifically ordered

- Board
- Fanless Chassis
- 2G DDR3 non ECC SO-DIMM memory
- 150W power adaptor
- SATA + power cable (custom made)
- 60G SSD Hard Disk
- Intel® Core™ i5-3610ME Processor (PGA) and Mobile Intel® QM77 Express Chipset Development Kit Quick Start
- DVD installer driver

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2 Features

Figure 1. Block Diagram

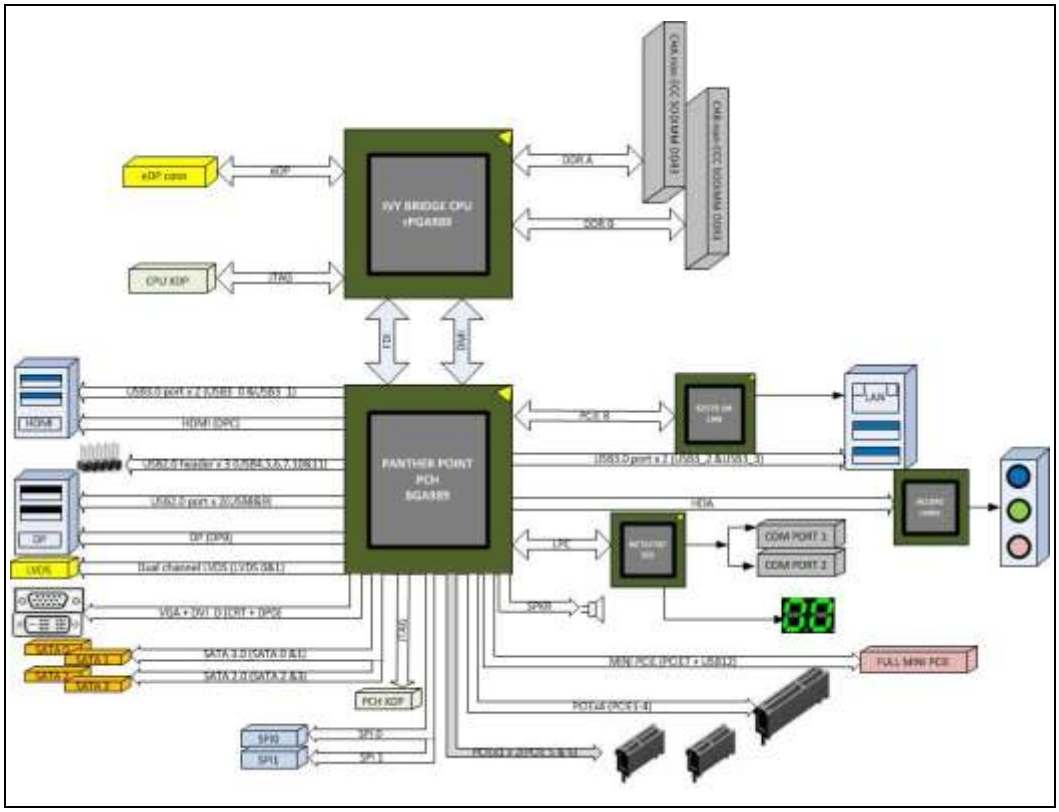

Table 3. Feature set summary

Feature Description	Implementation	Comments
Processor	Ivy Bridge-Mobile processor supported in 989pin rPGA package	Ci5 Ivy Bridge 2C CR i5-3610ME 2.7G 3M Refdes on board: U5E1
Chipset	Panther Point- M	989-pin FCBGA Foot-Print; Refdes on board: U3D1
Memory	2x DDR3 SODIMM non ECC slots	Maximum capacity of 8GB using 4Gb technology; Minimum capacity of 256 MB using 512 Mb technology; Supports DDR3 frequency of up to 1600 MT/s with Ivy Bridge; Refdes on Board: DIMM1, DIMM 2

Feature Description	Implementation	Comments
SIO	NCT6776F	Nuvoton LPC I/O; Refdes on Board:U2D1
Video	1x 24-bit dual channel LVDS Interface	There are 3 connectors on board: 2 LVDS 20pins data connector Redfes on Board:J3C2, J3C1 1 LVDS backlight connector Redfes on Board:J4C2
	Embedded Display Port (eDP)	x4 eDP (18bit, single channel) from CPU connected to onboard eDP connector Redfes on Board:J3F1
	Display Port	Connect from chipset Port B to DP connector Redfes on Board:J3A2
	HDMI	Connect from chipset Port C to HDMI connector Redfes on Board:J4A1
	DVI-D	Connect from chipset Port D to DVI-D connector Refdes on board: J6A1
	SDVO	N/A in this Development Kit
	CRT	On Board right-angled CRT Connector Refdes on board: J6A1
PCI Express	8x PCIe lanes from Panther Point	PCI Express 2.0 Compliance, 2.5GT/s PCIe1-4 to PCIe x4 slot Refdes on board: J1B2
		PCIe5, PCIe 6 to 2 PCIe x1 slot (optional) Refdes on board: J1F2, J1A1
		PCIe7 to WLAN mini PCIe Refdes on board: J6R1
		PCIe8 to 82579 (Lewisville) LAN
On-Board LAN	82579 (Lewisville) PHY supported	Refdes on board: U2C1
BIOS (SPI)	SPI flash devices	Support for multi-vendor SPI; 2x 4MB SOIC-8 parts provided on board. Refdes on board: U2E4, U2E3
		Support multi package (SOIC-8 & SOIC-16) (optional) Refdes on board: U2E2, U2E1
SATA	2x SATA III Ports	SATA connector with 4 pin power header on board SATA III connector

Feature Description	Implementation	Comments
	2x SATA II Ports	Refdes on board: SATA2F3, SATA2F2
		SATA II connector; Refdes on board: SATA2F1, SATA1F1
		SATA power header; Refdes on board: J3G1,J3G2,J4G1,J4G2
USB	4x USB 3.0 Ports 14x USB 2.0 Ports	2 Dual USB3.0 connector:USB0-USB3 Refdes on board: J5A1, J3A1 1 Dual USB2.0 connector: USB8-9 Refdes on board: J3A2 3 Dual USB2.0 header: USB4-7,10-11 Refdes on board: J2G1, J2G2, J2G3
		USB12 to WLAN mini PCIe Refdes on board: J6R1
LPC		1x LPC Slot connect to SIO and TPM headers
Clocks	Fully integrated Clocking	
RTC	Battery-backed real time clock	
Processor Voltage Regulator	IMVP-7 compliant CPU and GFX VRs	ISL95832, 3+2 VR
Power Supply	Mobile Mode	150W power supply adaptor
Debug Interfaces	CPU and PCH XDP Connector	On board CPU and PCH XDP Ports
Form Factor	MINI- ITX	

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3 Power management

3.1 Power Management States

Table 4 lists the power management states that have been defined for the platform. The Controller Link (CL) operates at various power levels, called M-states.

Table 4. Power Management States Description

State	Description
G0/S0/C0	System Up and Running
G0/S0/C3	Deep Sleep
G1/S3	Suspend To RAM (all switched rails are turned off)
G1/S4	Suspend To Disk
G2/S5	Soft Off
G3	Mechanical Off

Table 5. Development Kit states

NET	VOLTAGE LEVEL	S0/M0	S3/M3	S4/M3	S5/M3	G3	DSW
V3P3_DSW	3.3V						ON
V3P3_RTC	3.3V	ON	ON	ON	ON	ON	OFF
V5_A	5V	ON	ON	ON	ON	OFF	OFF
V3P3_A	3.3V	ON	ON	ON	ON	OFF	OFF
V3P3_M	3.3V	ON	ON	ON	ON	OFF	OFF
V1P05_M	1.05V	ON	ON	ON	ON	OFF	OFF
V5	5V	ON	OFF	OFF	OFF	OFF	OFF
V3P3	3.3V	ON	OFF	OFF	OFF	OFF	OFF
V1P8	1.8V	ON	OFF	OFF	OFF	OFF	OFF
V1P5	1.5V	ON	ON	OFF	OFF	OFF	OFF
V0P85	0.85V-0.95V	ON	OFF	OFF	OFF	OFF	OFF
V0P75	0.75V	ON	OFF	OFF	OFF	OFF	OFF
V1P05	1.05V	ON	OFF	OFF	OFF	OFF	OFF

NET	VOLTAGE LEVEL	S0/M0	S3/M3	S4/M3	S5/M3	G3	DSW
V1P05_VTT	1.05V	ON	OFF	OFF	OFF	OFF	OFF
VCC_GFXCORE	0.4-1.25V	ON	OFF	OFF	OFF	OFF	OFF
VCC_CORE	0.35-1.5V	ON	OFF	OFF	OFF	OFF	OFF

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4 Reference Board Summary

The following figures show the major components and jumpers and Table 6 gives a brief description of each component.

Figure 2. Board Layout - Top view

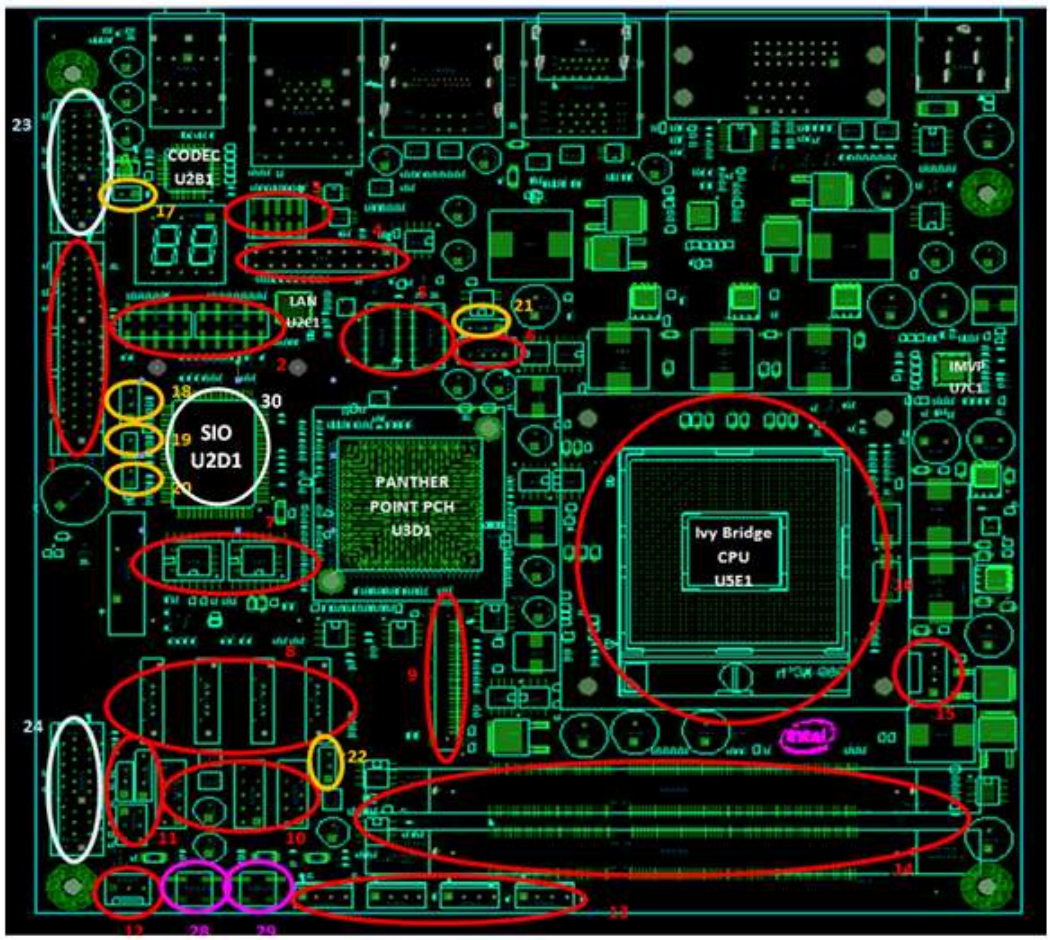

Figure 3. Board Layout – Bottom view

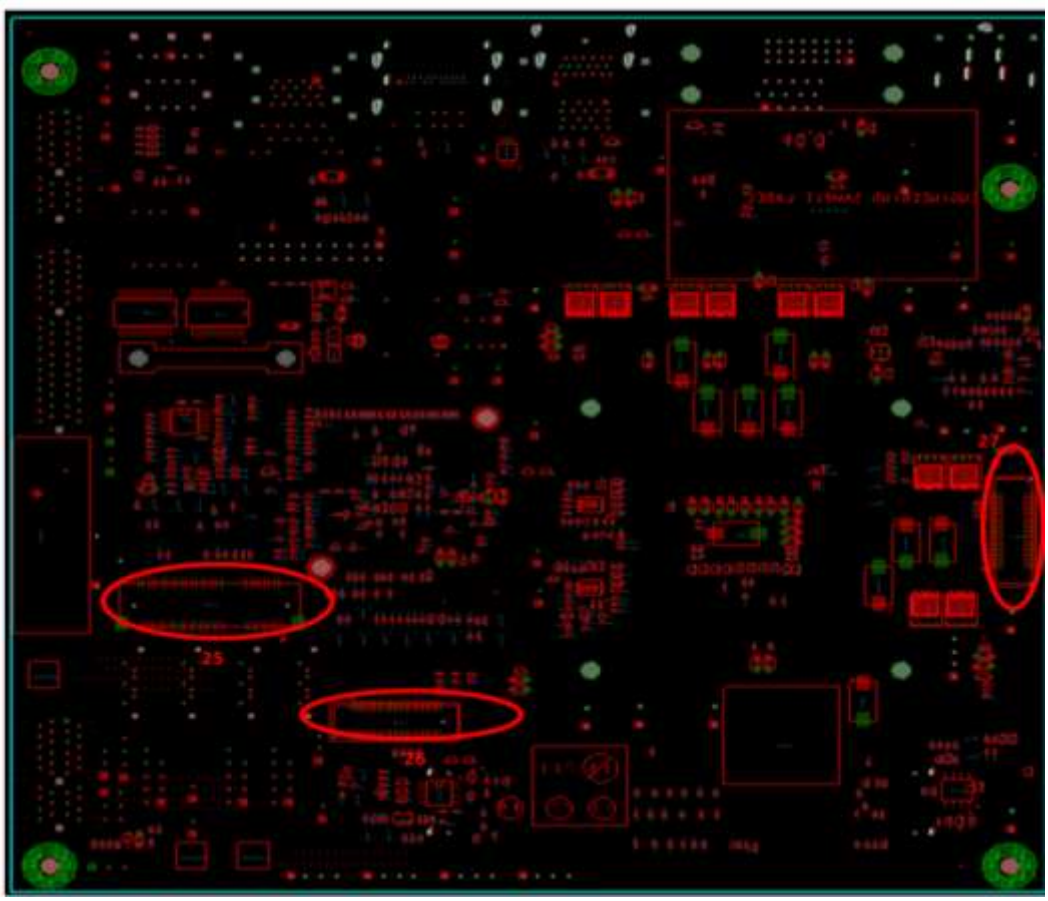

Table 6. Components list

Item	Description	Refdes	Item	Description	Refdes
1	PCIe x4 VT connector	J1B2	16	CPU socket	XU5E1
2	COM header	J2C1 (COM 1) J1C1 (COM 2)	17	SPI Flash Safety Performance Jumper Setting	J1B1
3	GPIO header	J2B1	18	Enable the Operating Voltage of LVDS and Embedded Panel Jumper Setting	J1D1
4	TPM header	J3B1	19	Clear/Keep ME Register Jumper Setting	J1D2
5	LVDS data connector	J3C2 (LVDSA) J3C1 (LVDSB)	20	Clear/Keep CMOS Jumper Setting	J1D3
6	LVDS backlight connector	J4C2	21	LVDS input voltage Jumper Setting	J4C1
7	SPI chip	U2E4 (SPI 0) U2E3 (SPI 1)	22	EDP input voltage Jumper Setting	J3F2
8	SATA connector	SATA1F1 (SATA2.0) SATA2F1 (SATA2.0) SATA2F2 (SATA3.0) SATA2F3 (SATA3.0)	23	PCIe x1 VT connector (empty)	J1A1
9	Embedded Display Port (EDP) Connector	J3F1	24	PCIe x1 VT connector (empty)	J1F2
10	Dual USB 2.0 header	J2G1 J2G2 J2G3	25	WLAN mPCIe	J6R1
11	Front Panel header	J1G1 (1-4: PWR BTN 2-5: RST 2-6: HDD LED) J1G2 (PWR LED) J1G3 (SPK OUT)	26	PCH XDP	J5T1
12	SYS Fan	J1G4	27	CPU XDP	J1R1
13	SATA power header	J3G1 J3G2 J4G1 J4G2	28	Reset button	SW1G1
14	204pin DDR3 non ECC SODIMM Connector	DIMM1 (CH A) DIMM2 (CH B)	29	Power push button	SW2G1
15	CPU Fan	J7F1	30	SIO	U2D1

4.1 Connectors

4.1.1 Back Panel Connectors

Figure 4. Back Panel Connectors

4.1.2 Configuration Settings

Caution: Do not move jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumper settings or damage may occur to the board.

Table 7. J1D3-Clear/Keep CMOS Setting

Setup	Function
0-1	Default
1-2 (Short)	Clear the contents of CMOS and all BIOS settings will restore to factory default values.

To restore the BIOS setting:

(1) Turn off the board and unplug the power cord

(2) Short the header on J1D3 with a jumper for a few seconds (that is, connect pin 1 and pin 2), then disconnect the jumper on that header. Remember that this header is not shorted with a jumper by default.

(3) Turn on the board

Table 8. J1D2-Clear/Keep ME Register Setting

Setup	Function
0-1 Open	Default
1-2 (Short)	Clear the contents of ME RTC register and all the settings will restore to factory default values.

To restore the ME setting:

(1) Turn off the board and unplug the power cable

(2) Short the header on J1D2 with a jumper for a few seconds (that is, connect pin 1 and pin 2), then disconnect the jumper on that header. Remember that this header is not shorted with a jumper by default.

(3) Turn on the board

Table 9. J1B1-Flash descriptor security override

Setup	Function
0-1	Enable ME function and disable on-line refresh BIOS. (Default)
1-2 (Short)	Disable ME function while enable on-line refresh BIOS.

Table 10. J1D1-Enable the Operating Voltage of LVDS and eDP

Setup	Function
1-2	Enabled LVDS
2-3	Enabled EDP (Default)

Table 11. J4C1-Select LVDS panel Operating Voltage

Setup	Function
1-2	3.3V (Default)
2-3	5V

Table 12. J3F2-Select eDP panel Operating Voltage

Setup	Function
1-2	3.3V (Default)
2-3	5V

4.1.3 Header Pinout Configuration

Table 13. J2G1/J2G2/J2G3 USB Port

There are three 2x5 Pin dual USB 2.0 headers on board.

Pin	Signal Name	Pin	Signal Name
1	5V	2	5V
3	USB1_Data-	4	USB2_Data-
5	USB1_Data+	6	USB2_Data+
7	GND	8	GND
9	NA	10	GND

Table 14. J2C1/J1C1Serial Port

- COM1: J2C1
- COM2: J1C1

Pin	Signal Name	Pin	Signal Name
1	DCD#	2	RXD
3	TXD	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	NC

Note: Please make sure the PCH CLKRUN# logic is "disable" OR Serial IRQ mode is "continuous" in BIOS SETUP to enable the serial port.

Table 15. J2B1 GPIO Header

Pin	Signal Name	Pin	Signal Name
1	GPIO1	2	GPIO5
3	GPIO2	4	GPIO6
5	GPIO3	6	GPIO7
7	GPIO4	8	GPIO8
9	GND	10	NC

Note: The pins for GPIO are bi-directional signals. The factory default value is that Pins 1, 3, 5 and 7 are for TTL input while Pins 2, 4, 6 and 8 are for CMOS output. The factory default status is high level while the voltage range for IO signals is 0-5V.

Table 16. J3B1- TPM Pin Header

Pin	Signal Name	Pin	Signal Name
1	CLOCK	2	GND
3	LPC_FRAME-	4	NC
5	PLT_RST-	6	V5
7	LPC_AD3	8	LPC_AD2
9	V3P3	10	LPC_AD1
11	LPC_AD0	12	GND
13	SMB_CLK	14	SMB_DATA
15	V3P3_A	16	SERIRQ
17	GND	18	CLKRUN
19	SUS_SATA-	20	LPC_DRQ0-

Recommended TPM: Nuvoton NPCT42x

Table 17. J4C2-LVDS Backlight Control Connector

Pin	Signal Name
1	V12
2	L_BKLT_CTL
3	L_BKLTEN
4	GND

V12: Backlight Power (12V)

L_BKLT_CTL: Backlight Control (voltage amplitude is between 0V-3.3V while the duty cycle is between 0% ~ 100%)

L_BKLTEN: Backlight Enable (Active High)

4.1.3.1 J3C2/J3C1- Dual Channel LVDS Data Connector

This Development Kit provides one dual-channel 24bit LVDS connector.

- LVDS 1: J3C2
- LVDS 2: J3C1

If single channel 18-bit LVDS screens are adopted, the LVDS data cable must connect to LVDS 1 only.

Note: LVDSA_X indicates to dual scan the odd line while LVDSB_X indicates to dual scan the even line.

Table 18. J3C2 LVDS1 Connector

Pin	Signal Name	Pin	Signal Name
1	LVDSA_D0+	2	LVDSA_D0-
3	GND	4	GND
5	LVDSA_D1+	6	LVDSA_D1-
7	GND	8	GND
9	LVDSA_D2+	10	LVDSA_D2-
11	GND	12	GND
13	LVDSA_CLK+	14	LVDSA_CLK-
15	GND	16	GND
17	LVDSA_D3+	18	LVDSA_D3-
19	VDD_LCD	20	VDD_LCD

Table 19. J3C1 LVDS2 Connector

Pin	Signal Name	Pin	Signal Name
1	LVDSB_D0+	2	LVDSB_D0-
3	GND	4	GND
5	LVDSB_D1+	6	LVDSB_D1-
7	GND	8	GND
9	LVDSB_D2+	10	LVDSB_D2-
11	GND	12	GND
13	LVDSB_CLK+	14	LVDSB_CLK-
15	GND	16	GND
17	LVDSB_D3+	18	LVDSB_D3-
19	LCD_VDD	20	LCD_VDD

4.1.3.2 Embedded Display Port (eDP) connector

This Development Kit provides one 18bit eDP connector.

Note: This Development Kit supports either LVDS or eDP and both cannot be enabled at the same time. It needs to set in the BIOS SETUP and select J1D1 jumper (Enable the Operating Voltage of LVDS and eDP) to select which interface is going to be used.

Table 20. J3F1 Embedded Display Port (eDP) Connector

Pin	Signal Name	Pin	Signal Name
1	VCC(3.3V)	23	EDP0_TXN
2	VCC(3.3V)	24	EDP0_TXP
3	VCC(3.3V)	25	GND
4	VCC(3.3V)	26	EDP_AUXP
5	VCC(3.3V)	27	EDP_AUXN
6	GND	28	NC
7	GND	29	3.3V
8	GND	30	NC
9	GND	31	V12_EDP (12V)
10	EDP_HPD	32	NC
11	NC	33	GND
12	NC	34	5V
13	GND	35	L_CTRL_CLK
14	EDP3_TXN	36	L_BKLT_CTL
15	EDP3_TXP	37	L_BKLTEN
16	GND	38	V12_EDP (12V)
17	EDP2_TXN	39	3.3V
18	EDP2_TXP	40	GND
19	GND	41	SMB_CLK_MAIN
20	EDP1_TXN	42	SMB_DATA_MAIN
21	EDP1_TXP	43	NC
22	GND	44	NC

4.1.3.3 Front Panel Status Indicating and Control Connector

Table 21. J1G3 Power Switch and HDD Indicator header

Pin	Signal Name	Pin	Signal Name
1	PWRBTN#	4	GND
2	GND	5	RESET#
3	SATA_LED-	6	5V

1-4: Power Button

2-5: Reset Button

3-6: Hard Drive LED indicator

Table 22. J1G1 Power Indicator Header

Pin	Signal Name
1	PWR_LED+
2	NC
3	GND

Table 23. J1G2 Speaker Output Header

Pin	Signal Name
1	SPEAKER
2	NC
3	GND
4	+5V

4.2 Power On and Reset Buttons

This Development Kit has two push-buttons, POWER and RESET. The POWER button enables/disables power to the entire board causing the board to boot or shut off. The RESET button forces all systems to warm reset.

The POWER button is located at SW2G1 and the RESET button is located at SW1G1

Description	Reference Designator
Power Button	SW2G1
Reset Button	SW1G1
Processor	U5E1

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