X540

10GBASE-T DUAL PORT ETHERNET CONTROLLER

REFERENCE DESIGN

TABLE OF CONTENTS

REVISION HISTORY

REV0.70 - PU/PD, TM_REXT, BG_REXT VALUES UPDATE, TM_REXT TIED TO 2.5V, ADD 3X FERRITE BEAD - SEE PAGE 9

REV0.95 - BG_REXT - 2KOHM, THERMAL DIODE, 2.5V FLASH, FILTER CAP - 6.8PF

REV0.99 - PIN MODIFIED RSVDM23_VCC2P5, RSVDD14_NC, ADDING PU OR PD OPTIONS TO RSVDK3_VSS, ADD PD TO NCSI_ARB_IN, CRYSTAL CAP CL1/CL2 CHANGE TO 18PF, RESISTORS VALUE PE_RBIAS0, PE_RBIAS1 CHANGE TO 3.01KOHM

REV0.995 - CONNECT RSVDM23_VCC2P5 TO PUP RES, MOVE PIN [J5] VCC0P65_J5 CLOSE TO VCC0P65_XX PINS

REV1.0 - ADDING INDUCTORS PART NUMBER ON PAGES: P9, P10, RSVDK3_VSS CONNECTED TO PD AS DEFAULT

REV1.05 – ADDING: INTEGRATED MAGNETIC ON PAGE 9, ADDING ADDITIONAL 1.2V RAIL BULK DECOUPLING, AND BULK DECOUPLING DISTRIBUTION NOTEs

REV1.2 - BULK DECOUPLING DISTRIBUTION NOTEs, K3 PD CLARIFICATION

REV1.25 – NCSI PD changed to 10KOHM

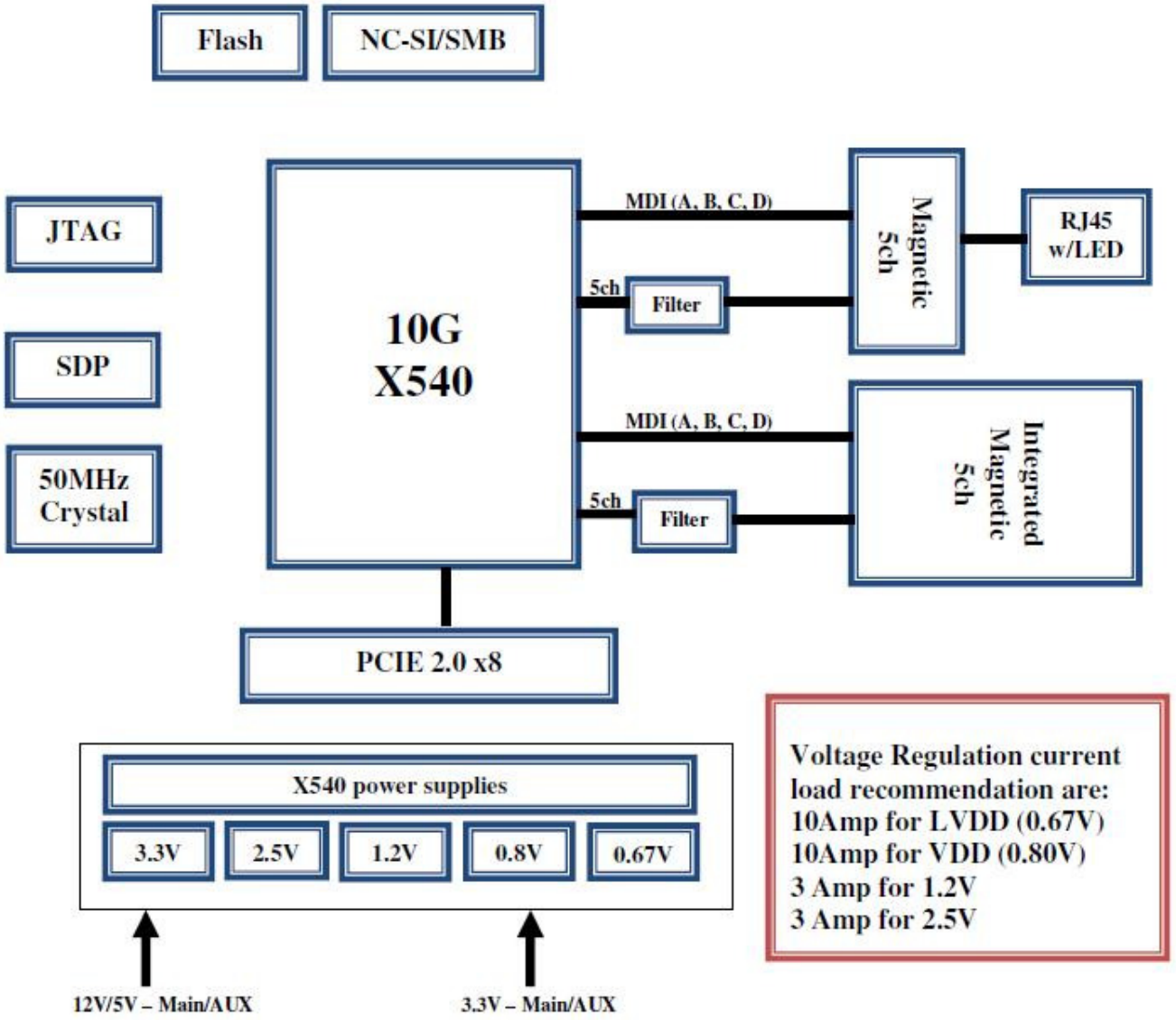
REV1.9 – Update BYPASS_POR signal to be connected to Pull-Down only

REV2.0 – MAIN_PWR_OK signal clarification

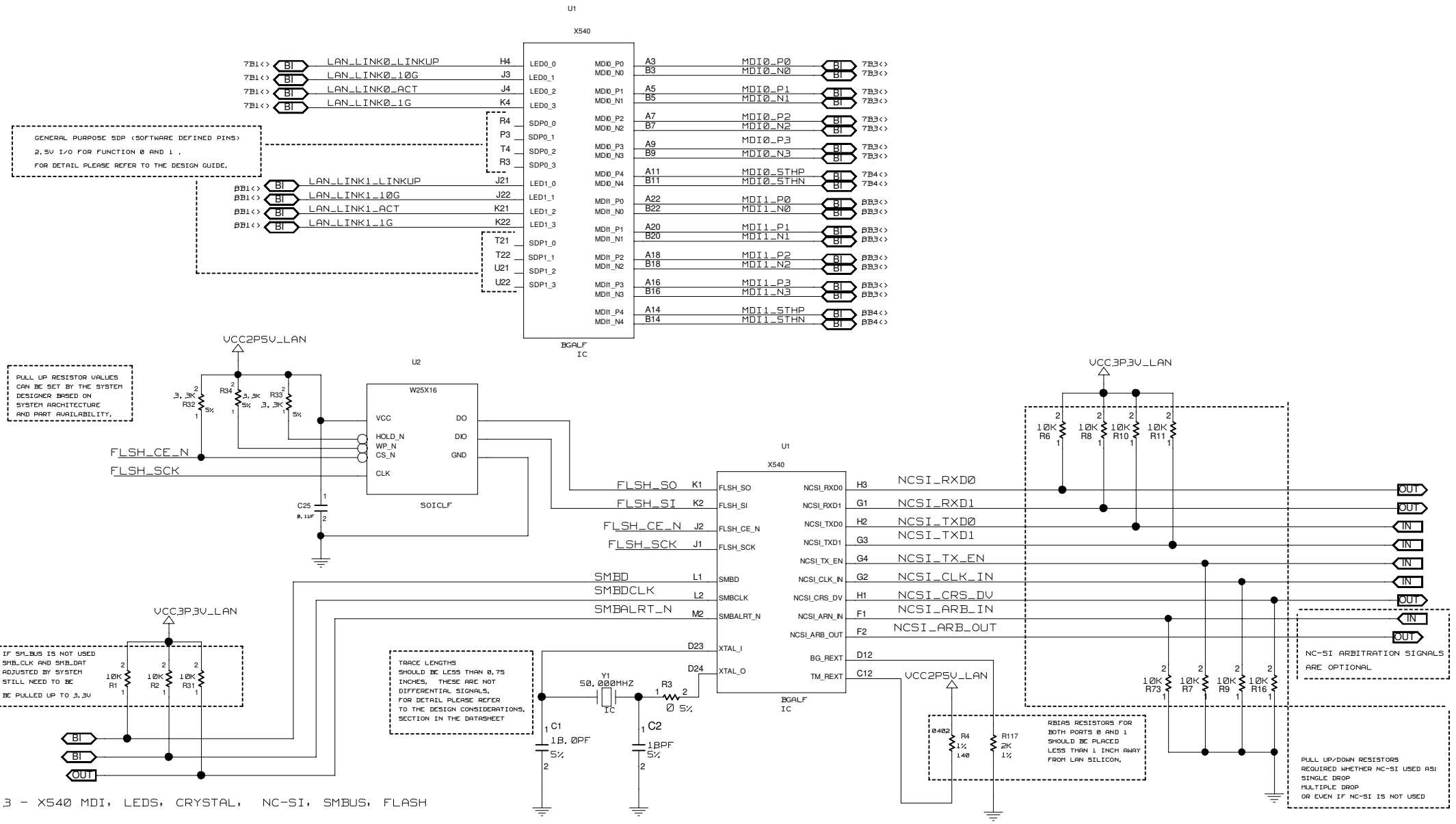
REV2.1 – Symbol update with VCC0P67_XX pins

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 1

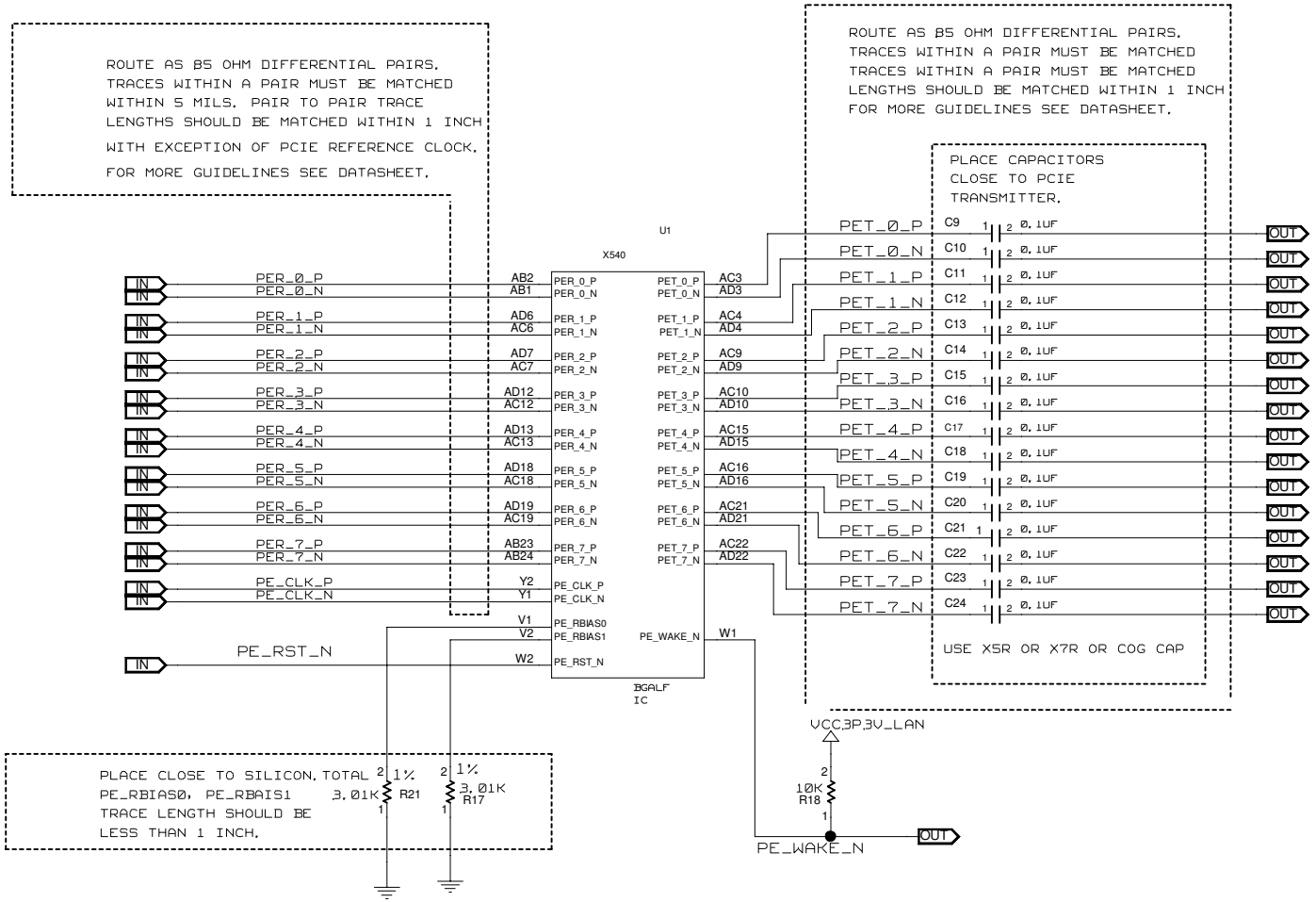
X540 Block Diagram



LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 2

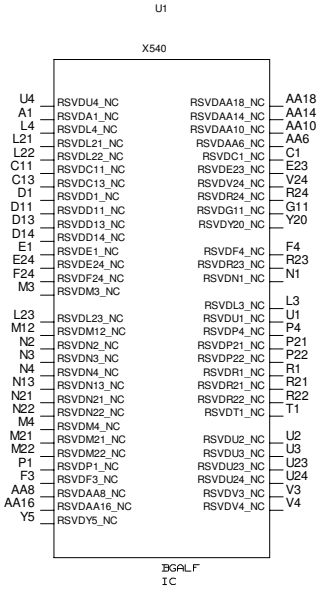


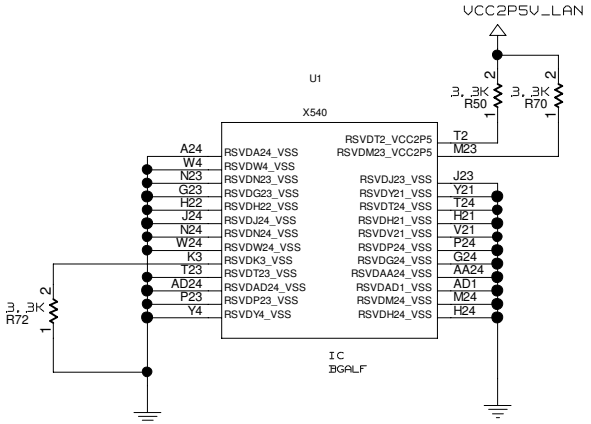
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 3



4 - X540 PCIE

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 4





RSRVD_VSS - SHOULD BE CONNECTED TO VSS
RSRVD_NC - SHOULD BE LEFT UNCONNECTED
RSRVD_VCC2P5 - SHOULD BE CONNECTED TO VCC2P5

5 - X540 RESERVED PINS

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 5

POWER ON RESET CONFIGURATION

USE INTERNAL POR AS DEFAULT

1. LAN_PWR_GOOD SIGNAL TO BE CONNECTED TO PULL UP
2. BYPASS_POR SIGNAL TO BE CONNECTED TO PULL DOWN

FOR EXTERNAL RESET USE:

1. LAN_PWR_GOOD SIGNAL ASSERTED BY THE SYSTEM (EXTERNAL POWER MONITORING SOLUTION)
2. BYPASS_POR SIGNAL TO BE CONNECTED TO PULL DOWN

FOR MORE DETAIL PLEASE CONSULT THE DATASHEET

THERMAL DIODE SIGNALS CAN BE CONNECTED TO REMOTE AND LOCAL SYSTEM TEMPERATURE MONITOR

SUGGESTED DEVICE ADM1032

VCC3P3V_MAIN

MAIN POWER GOOD. INDICATES THAT PLATFORM MAIN POWER IS UP. MUST BE CONNECTED EXTERNALLY.

VCC2P5V_LAN

R23 10K, R24 10K

IN LAN1_DIS_N

IN LAN0_DIS_N

STUFF IF AUX POWER IS AVAILABLE — R20 10K

AUX_PWR

STUFF IF AUX POWER IS NOT AVAILABLE — R22 10K EMPTY

R27 10K

IN LAN_PWR_GOOD

R28 10K, R39 10K

U1

X540

M1	SEC_EN	THERM_D1_P	G21
		THERM_D1_N	G22
L24	LAN_PWR_GOOD	PHY0_RVSL	T3
P2	AUX_PWR	PHY1_RVSL	V23
R2	MAIN_PWR_OK	TCK	Y22 JTCK
K24	LAN1_DIS_N	TDI	W22 JTDI
K23	LAN0_DIS_N	TDO	V22 JTDO
H23	BYPASS_POR	TMS	W21 JTMS
		TRST_N	W23 JTRST_N

IC BGALF

THERM_D1_P

THERM_D1_N

R30 10K, R43 3.30K, R44 10K

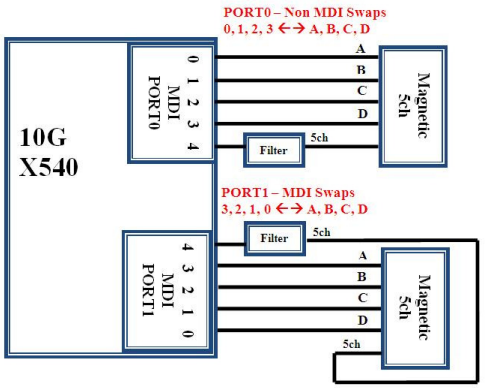
IN, IN, OUT, IN, IN

R29 470, R42 470

R61 3.3K, R62 3.3K

BYPASS_POR

R26 10K



PHY MDI LANE SWAPSL CONFIGURATION

DEFAULT CONFIGURATION – 0, 1, 2, 3 <-> A, B, C, D

CONNECT PHY0_RVSL SIGNAL TO GND VIA 3.3KOHM PULL DOWN

CONNECT PHY1_RVSL SIGNAL TO GND VIA 3.3KOHM PULL DOWN

MDI SWAPS CONFIGURATION – 3, 2, 1, 0 <-> A, B, C, D

CONNECT PHY0_RVSL SIGNAL TO 2.5V VIA 10KOHM PULL UP

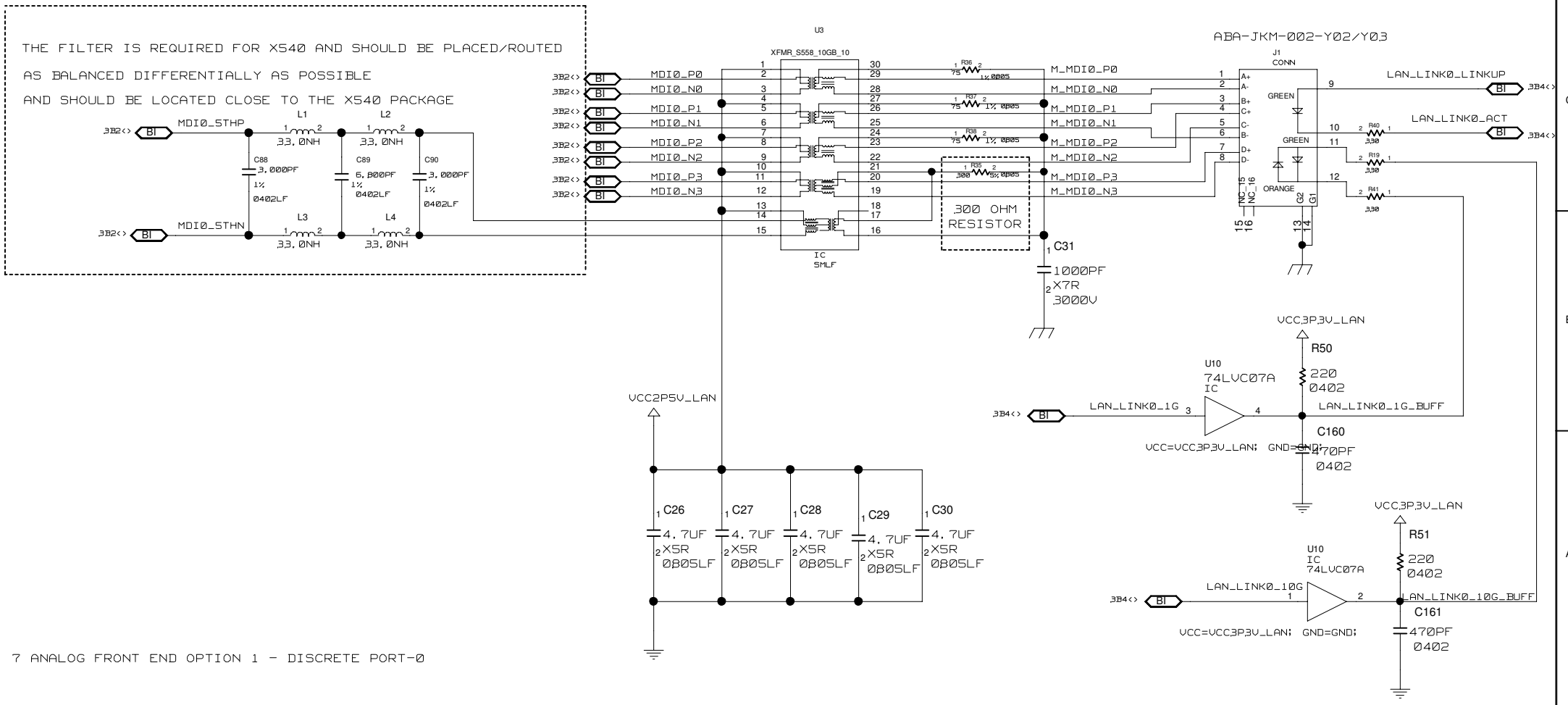
CONNECT PHY1_RVSL SIGNAL TO 2.5V VIA 10KOHM PULL UP

IF THE JTAG INTERFACE IS NOT CONNECTED TO THE SYSTEM JTRST_N SHOULD BE CONNECTED TO PD

6 – X540 JTAG, AUX POWER, LAN DISABLE, MAIN POWER OK, AND POWER ON RESET

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 6

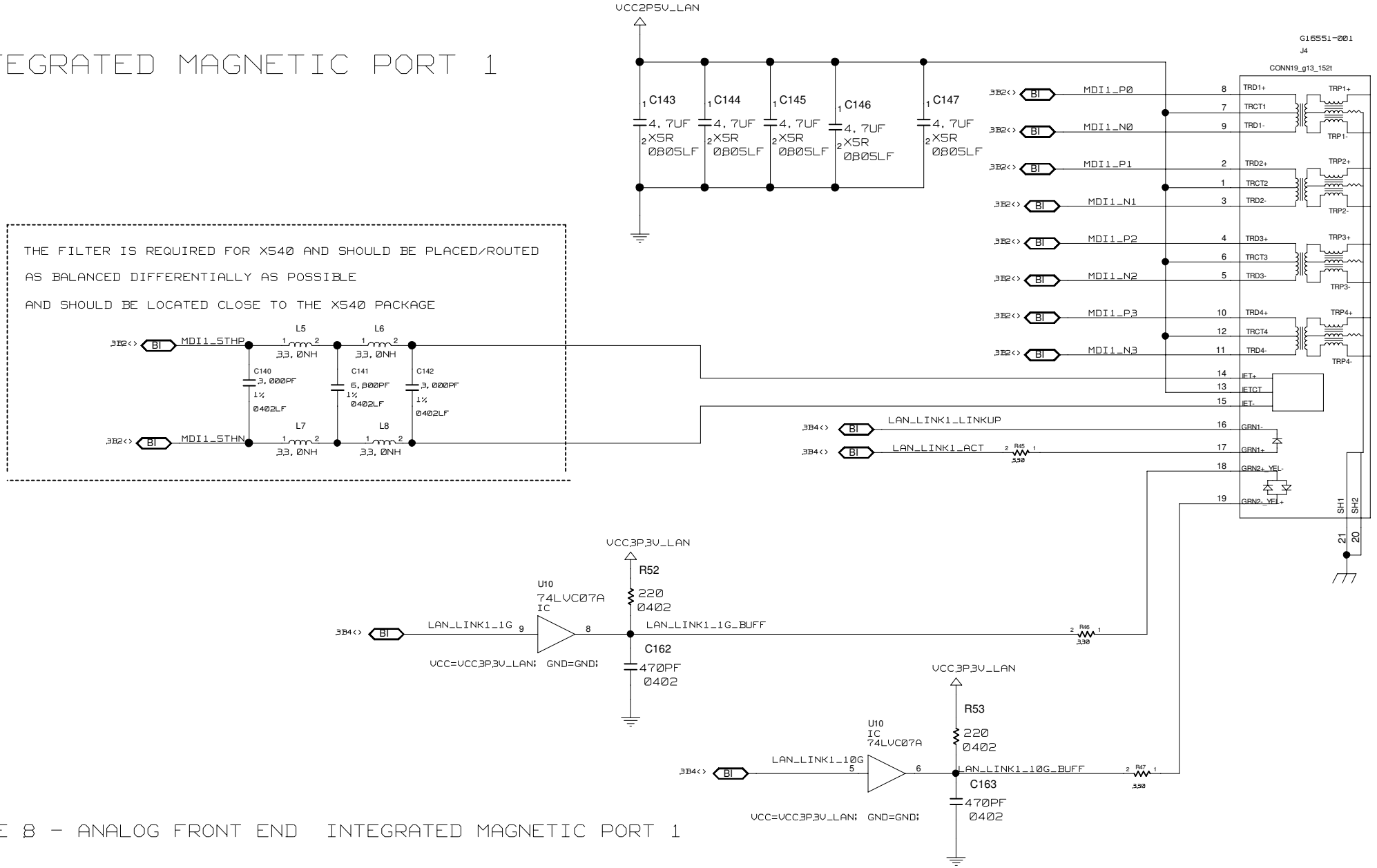
DISCRETE PORT-0



7 ANALOG FRONT END OPTION 1 - DISCRETE PORT-0

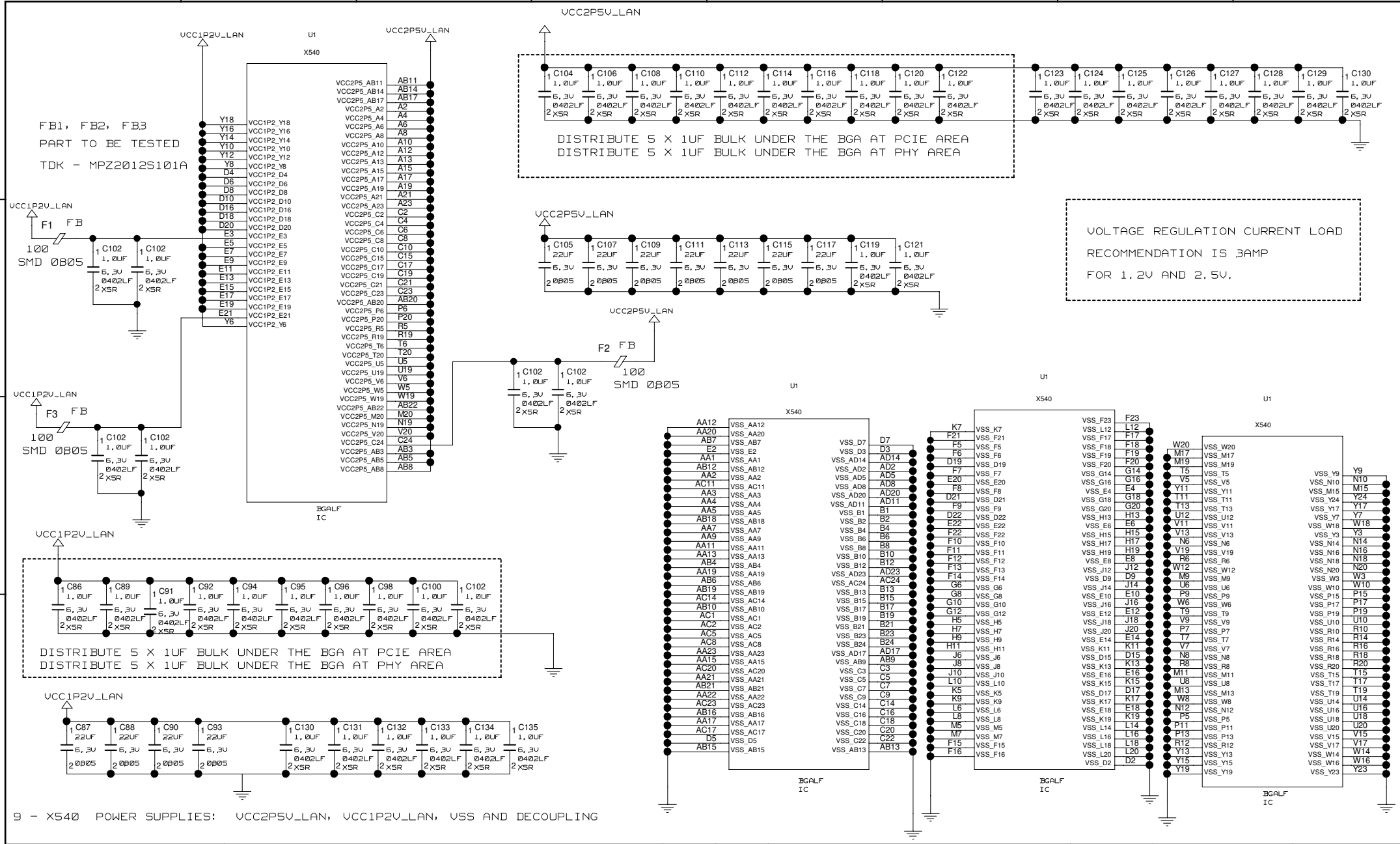
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 7

INTEGRATED MAGNETIC PORT 1



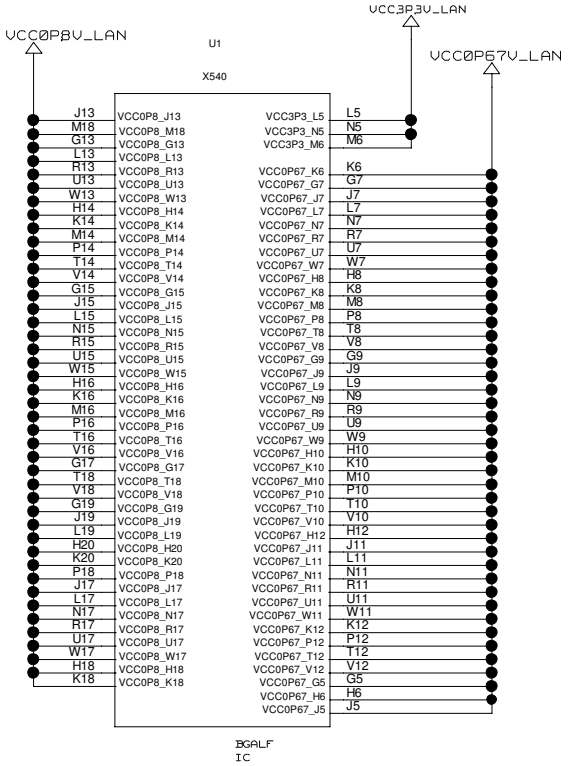
PAGE 8 – ANALOG FRONT END INTEGRATED MAGNETIC PORT 1

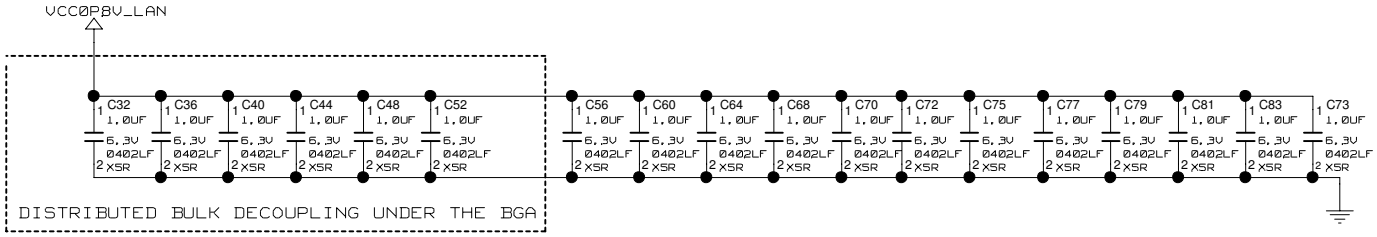
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 8

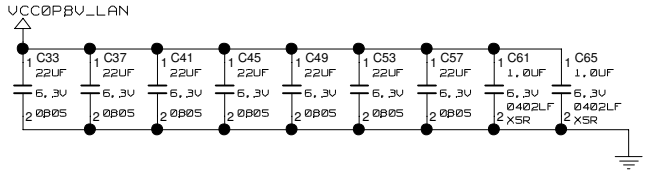


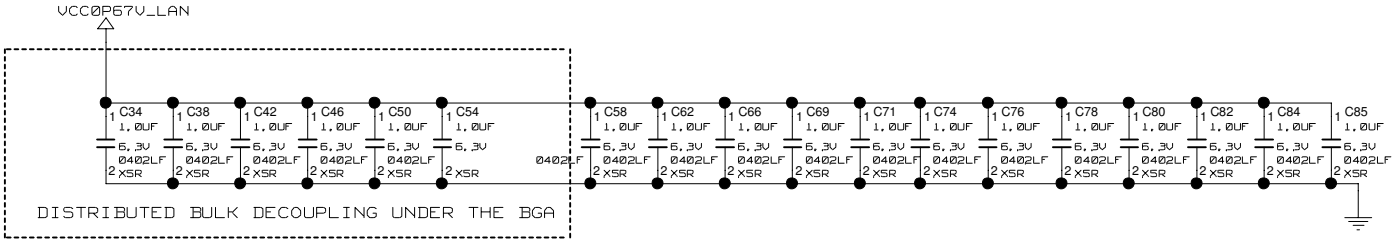
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: X540 REF SCHEMATIC	SIZE: B	CODE	DOCUMENT NUMBER	REV: 2.1	DATE: 11/27/2012	SHEET: 9

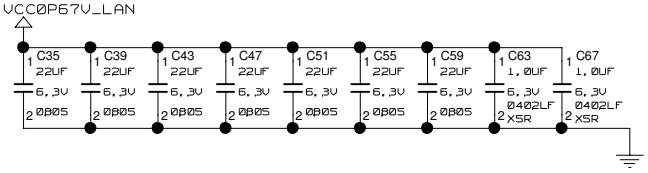
VOLTAGE REGULATION CURRENT LOAD
RECOMMENDATION IS 10AMP
FOR LVDD (0.65V) AND VDD (0.80V).

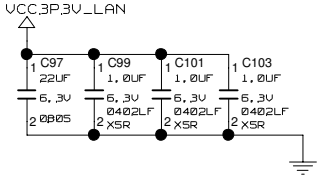












10 - X540 POWER SUPPLIES: VCC3P3, VCC0P8V_LAN, VCC0P67V_LAN, AND DECOUPLING

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540 REF SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 10