X540 / I350-BT2

REFERENCE DESIGN

X540: PCIE X8, 100/1000/10GB-T

I350-BT2: PCIE X4, 10/100/1000BASE-T

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REVISION HISTORY

REV0.95 - INITIAL RELEASE

REV0.96 - MODIFIED RSVDU23, RSVDU24 NAMES FOR I350

REV0.97 - CONNECT AUX_PWR SIGNAL TO X540VCC2P5V_I350VCC3P3V THROUGH 10KOM PU RES

REV0.99 - PIN MODIFIED RSVDM23_VCC2P5, RSVDD14_NC, ADDING PU OR PD OPTIONS TO RSVDK3_VSS, ADD PD TO NCSI_ARB_IN, CRYSTAL CAP CL1/CL2 CHANGE TO 18PF, RESISTORS VALUE PE_RBIAS0, PE_RBIAS1 CHANGE TO 3.01KOHM

REV0.995 - FOR X540 CONNECT RSVDM23_VCC2P5 TO PUP RES, AND PDOWN FOR I350, MOVE PIN [J5] VCC0P65_J5 CLOSE TO VCC0P65_XX PINS

REV1.0 - ADDING INDUCTORS PART NUMBER ON PAGES: P9, P10, RSVDK3_VSS CONNECTED TO PD AS DEFAULT

REV1.05 – ADDING: INTEGRATED MAGNETIC ON PAGE 9, ADDING ADDITIONAL 1.2V RAIL BULK DECOUPLING, AND BULK DECOUPLING DISTRIBUTION NOTEs

REV1.2 – BULK DECOUPLING DISTRIBUTION NOTES, M1, T2, M23, T3, V23 STUFFING OPTION CLARIFICATION

REV1.25 – NCSI PD changed to 10KOHM

REV1.9 – Update BYPASS_POR signal to be connected to Pull-Down only

REV2.0 – MAIN_PWR_OK signal clarification

REV2.1 – Symbol update with VCC0P67_XX pins

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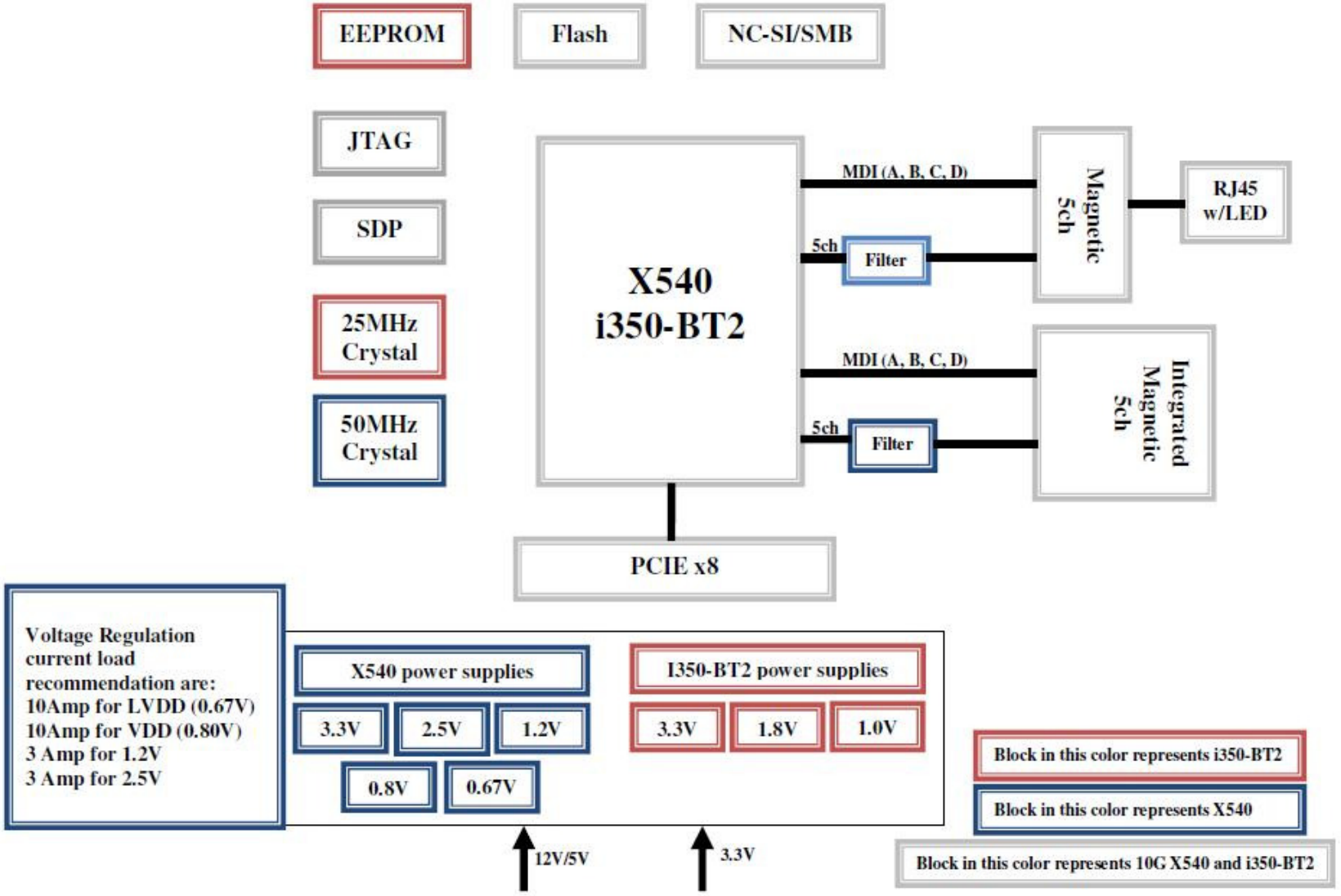
X540/i350-BT2 Block Diagram



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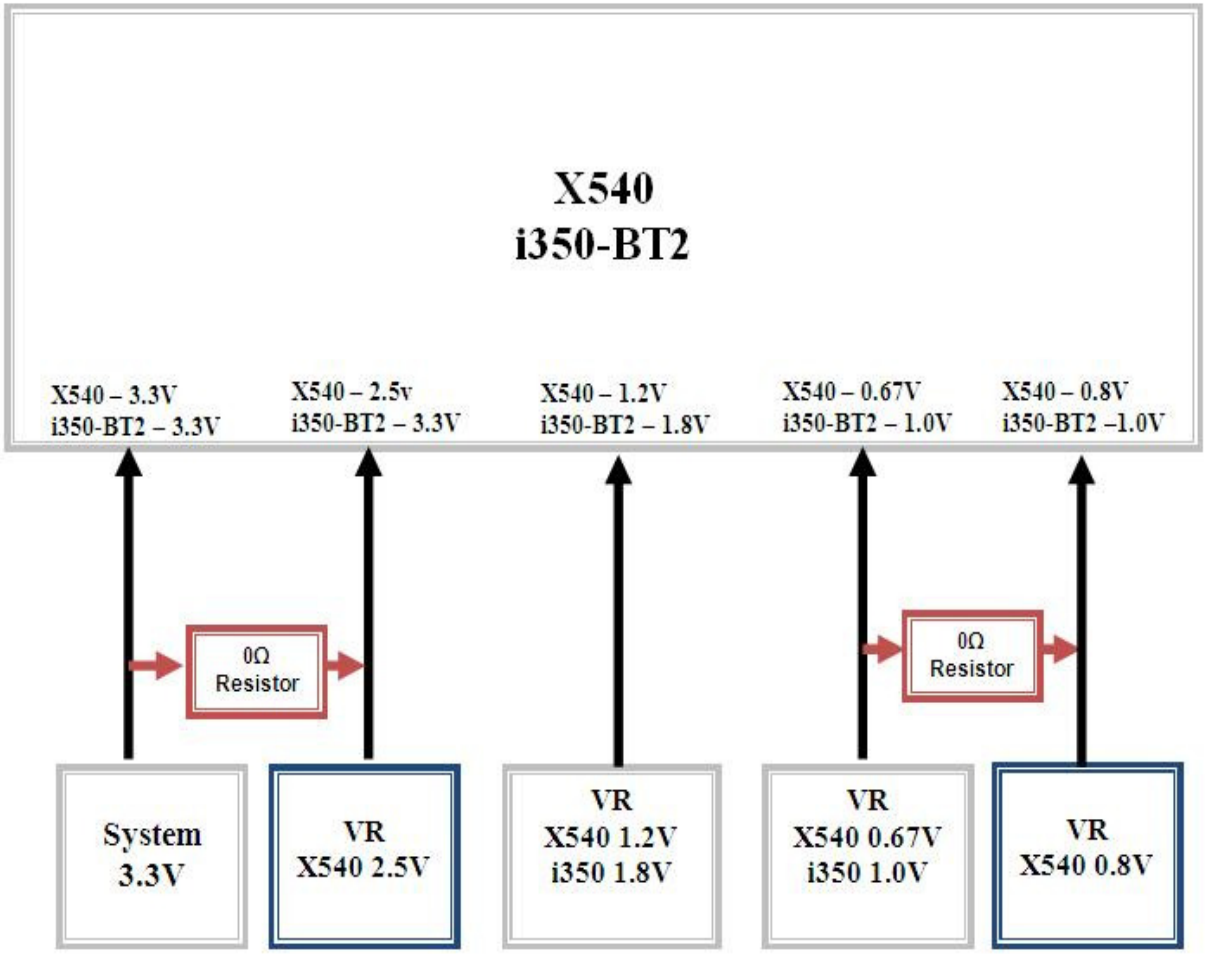
X540/i350-BT2 Voltage Rails Block Diagram

- System 3.3V rail
  - Common – connect 3.3V to X540/i350-BT2 ball pads
- 2.5V rail
  - X540 – connect 2.5V rail to X540 ball pads
  - i350-BT2 –
    - connect 0Ω resistor between 3.3V rail and 2.5V rail
    - disconnect X540 2.5V VR
    - Outcome – 3.3V connected to i350 3.3V ball pads
- 1.2V/1.8V rail
  - X540 – tuned VR voltage output to 1.2V and connect to X54
  - i350-BT2 - tuned VR voltage output to 1.8V and connect to i3
- 0.67V/1.0V rail
  - X540 – tuned VR voltage output to 0.67V and connect to X5
  - i350-BT2 - tuned VR voltage output to 1.0V and connect to i3
- 0.8V rail
  - X540 – connect 0.8V rail to X540 ball pads
  - i350-BT2 –
    - connect 0Ω resistor between 1.0V rail and 0.8V rail
    - Disconnect X540 0.8V VR
    - Outcome – 1.0V connected to i350 1.0v ball pads



Block in this color represents 10G X540 and i350

Block in this color represents X540

Block in this color represents i350

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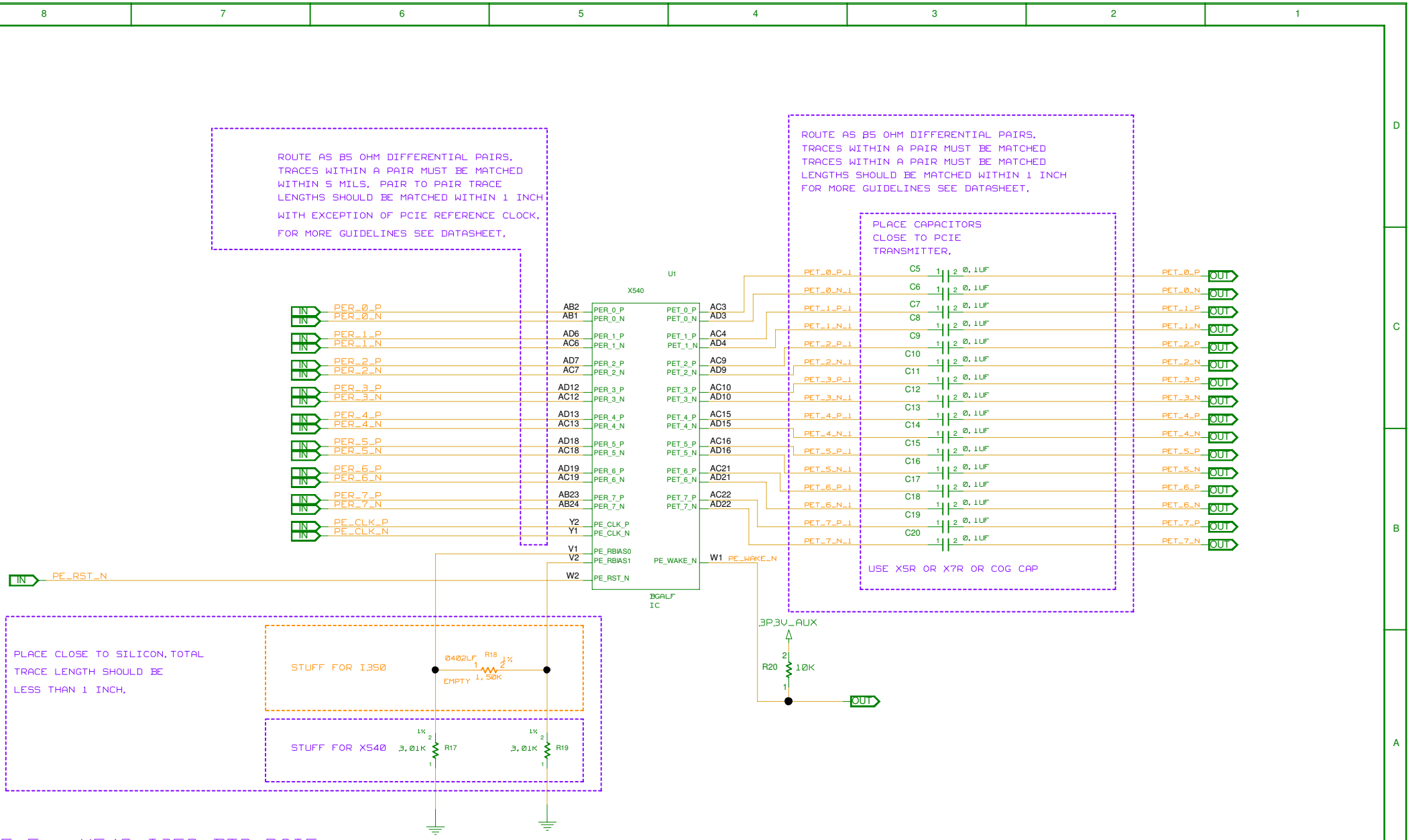

PAGE 5 - X540/I350-BT2 PCIE

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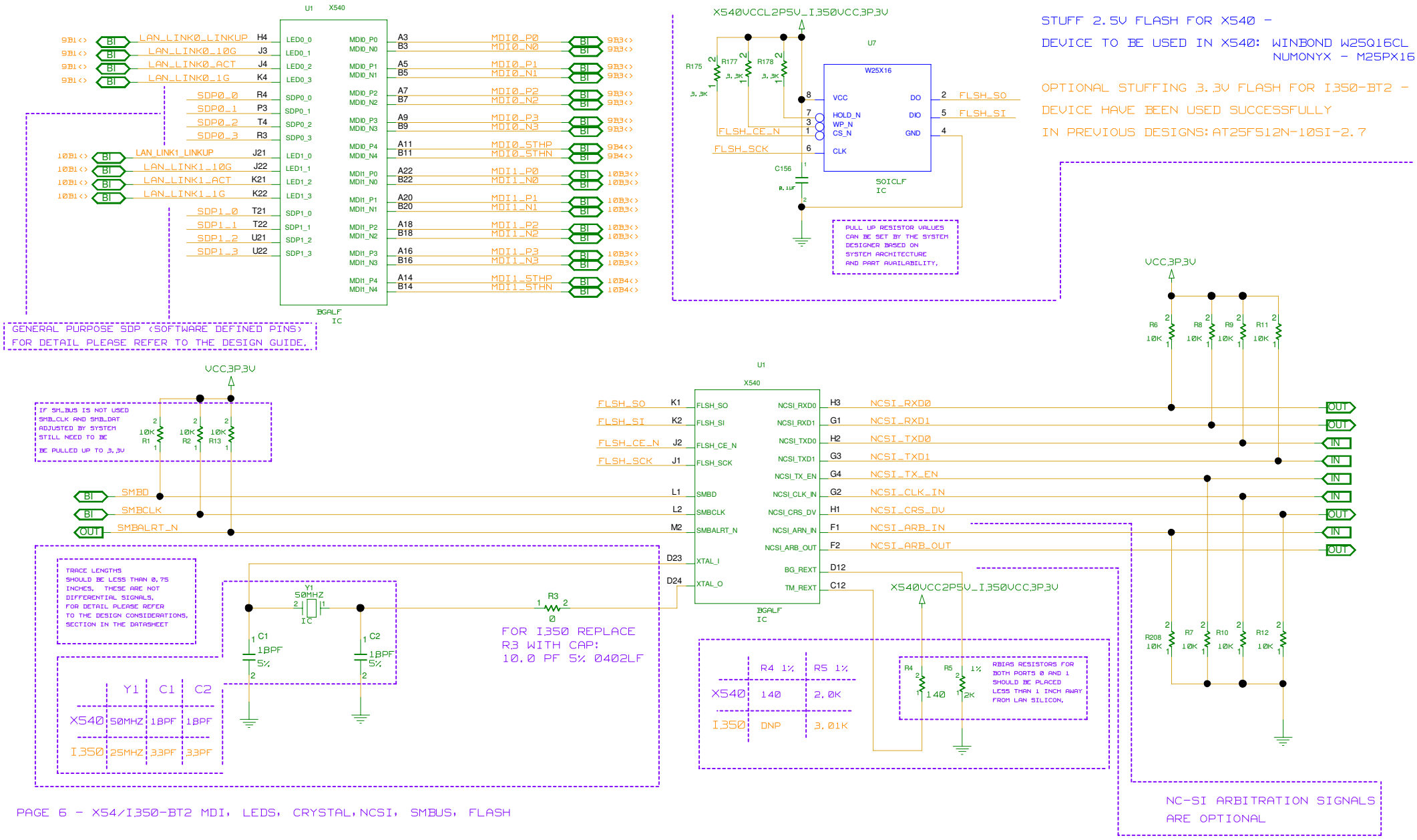
U1 X540
LAN_LINK0_LINKUP H4
LAN_LINK0_10G J3
LAN_LINK0_ACT J4
LAN_LINK0_1G K4
SDP0_0 R4
SDP0_1 P3
SDP0_2 T4
SDP0_3 R3
LAN_LINK1_LINKUP J21
LAN_LINK1_10G J22
LAN_LINK1_ACT K21
LAN_LINK1_1G K22
SDP1_0 T21
SDP1_1 T22
SDP1_2 U21
SDP1_3 U22
BGALF IC
GENERAL PURPOSE SDP (SOFTWARE DEFINED PINS)
FOR DETAIL PLEASE REFER TO THE DESIGN GUIDE.
X540VCCL2P5V_I.350VCC3P3V
U7
W25X16
VCC
HOLD_N
WP_N
CS_N
CLK
DO
DIO
GND
FLSH_SO
FLSH_SI
FLSH_CE_N
FLSH_SCK
SOICLF IC
PULL UP RESISTOR VALUES CAN BE SET BY THE SYSTEM DESIGNER BASED ON SYSTEM ARCHITECTURE AND PART AVAILABILITY.
STUFF 2.5V FLASH FOR X540 -
DEVICE TO BE USED IN X540: WINBOND W25Q16CL
NUMONYX - M25PX16
OPTIONAL STUFFING 3.3V FLASH FOR I.350-BT2 -
DEVICE HAVE BEEN USED SUCCESSFULLY
IN PREVIOUS DESIGNS: AT25F512N-10SI-2.7
VCC3P3V
IF SM_BUS IS NOT USED SMB_CLK AND SMB_DAT ADJUSTED BY SYSTEM STILL NEED TO BE BE PULLED UP TO 3.3V
SMBD
SMBCLK
SMBALRT_N
TRACE LENGTHS SHOULD BE LESS THAN 0.75 INCHES. THESE ARE NOT DIFFERENTIAL SIGNALS, FOR DETAIL PLEASE REFER TO THE DESIGN CONSIDERATIONS, SECTION IN THE DATASHEET
Y1 50MHZ IC
C1 18PF 5%
C2 18PF 5%
R3 0
FOR I.350 REPLACE R3 WITH CAP: 10.0 PF 5% 0402LF
Y1 C1 C2
X540 50MHZ 18PF 18PF
I.350 25MHZ 33PF 33PF
X540VCC2P5V_I.350VCC3P3V
R4 1% R5 1%
X540 140 2.0K
I.350 DNP 3.01K
RBIAS RESISTORS FOR BOTH PORTS 0 AND 1 SHOULD BE PLACED LESS THAN 1 INCH AWAY FROM LAN SILICON.
NCSI_RXD0 NCSI_RXD1 NCSI_TXD0 NCSI_TXD1 NCSI_TX_EN NCSI_CLK_IN NCSI_CRS_DV NCSI_ARB_IN NCSI_ARB_OUT
BG_REXT TM_REXT
NC-SI ARBITRATION SIGNALS ARE OPTIONAL
PAGE 6 - X54/I.350-BT2 MDI, LEDS, CRYSTAL, NCSI, SMBUS, FLASH
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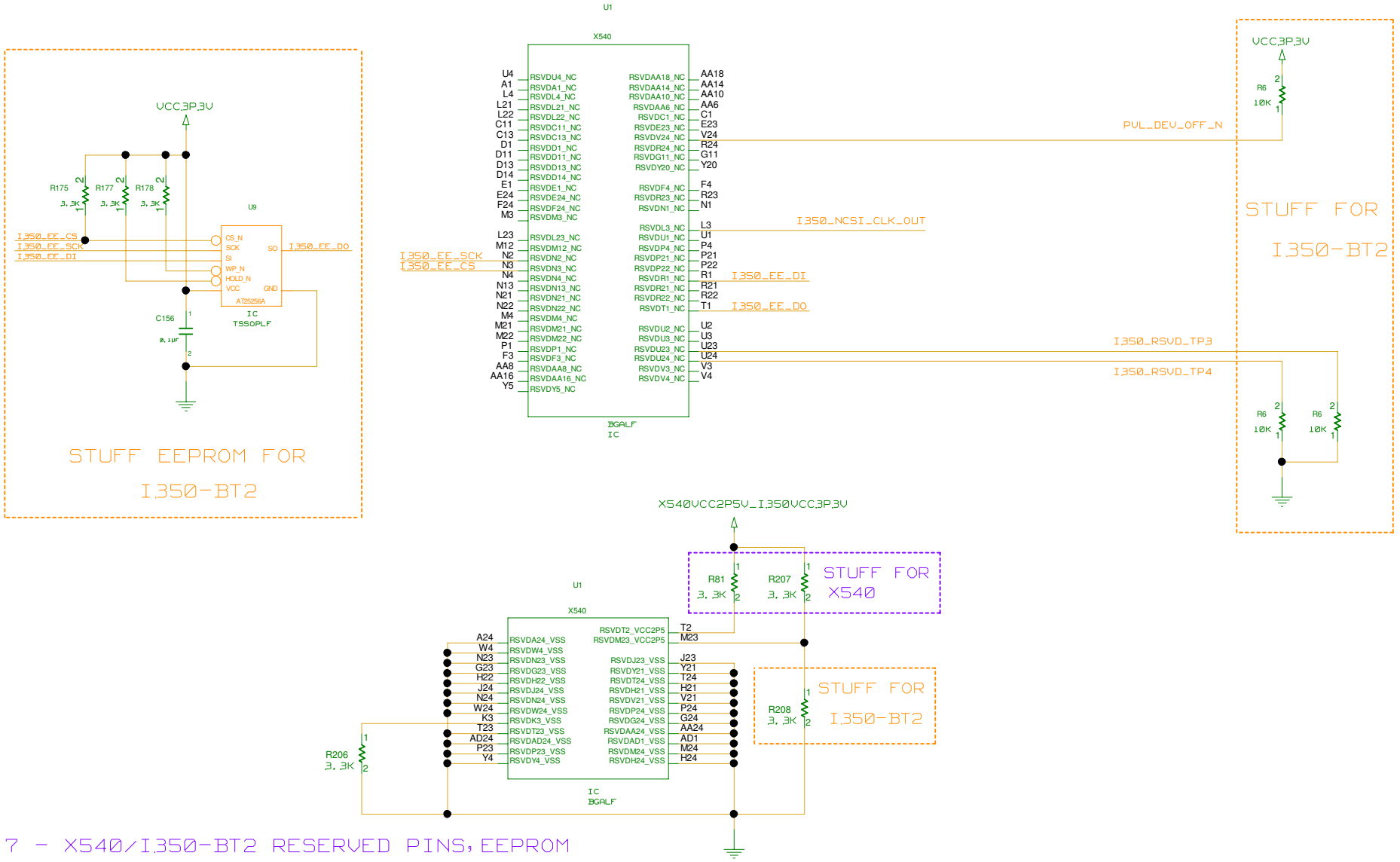

PAGE 7 - X540/I350-BT2 RESERVED PINS, EEPROM

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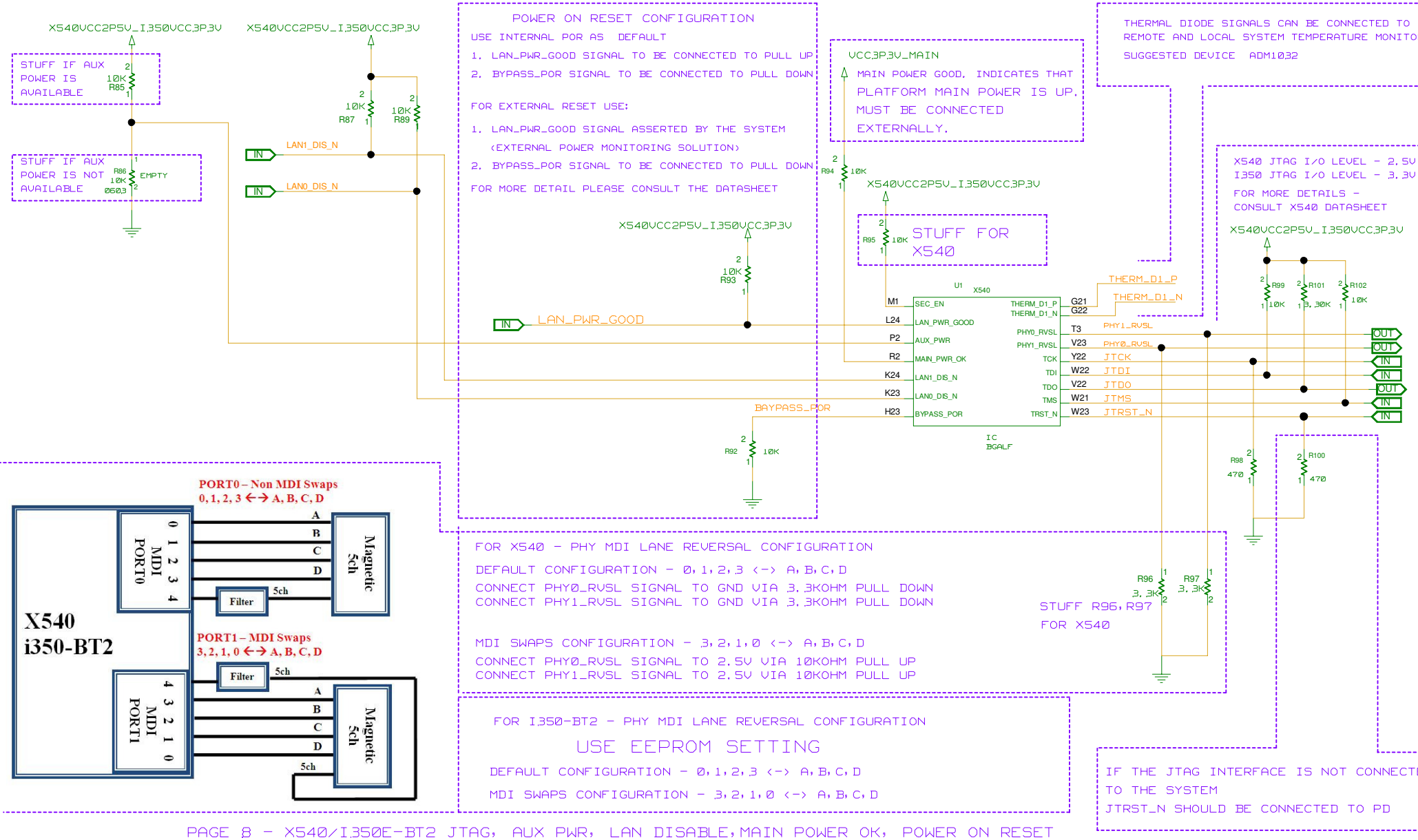

PAGE 8 - X540/I350E-BT2 JTAG, AUX PWR, LAN DISABLE, MAIN POWER OK, POWER ON RESET

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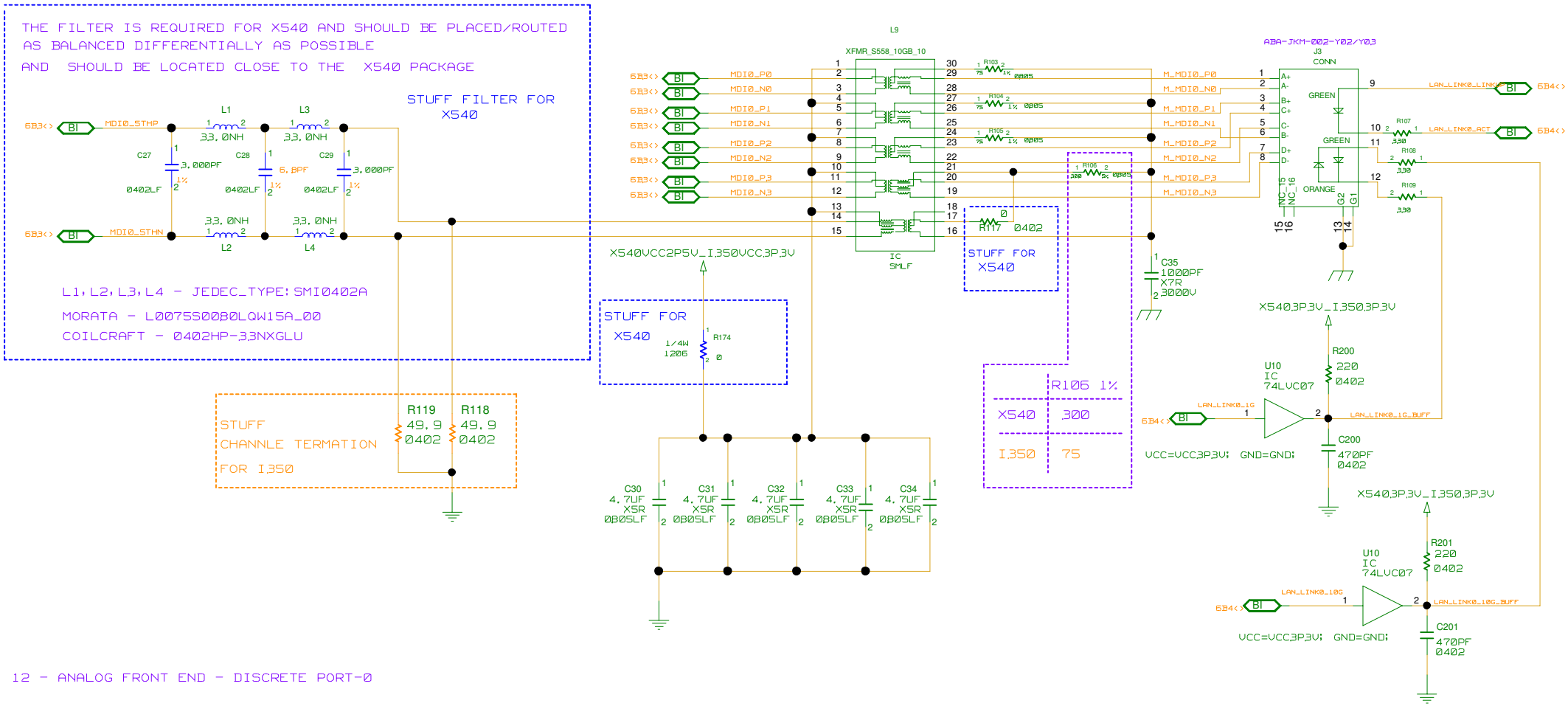
DISCRETE - PORT 0



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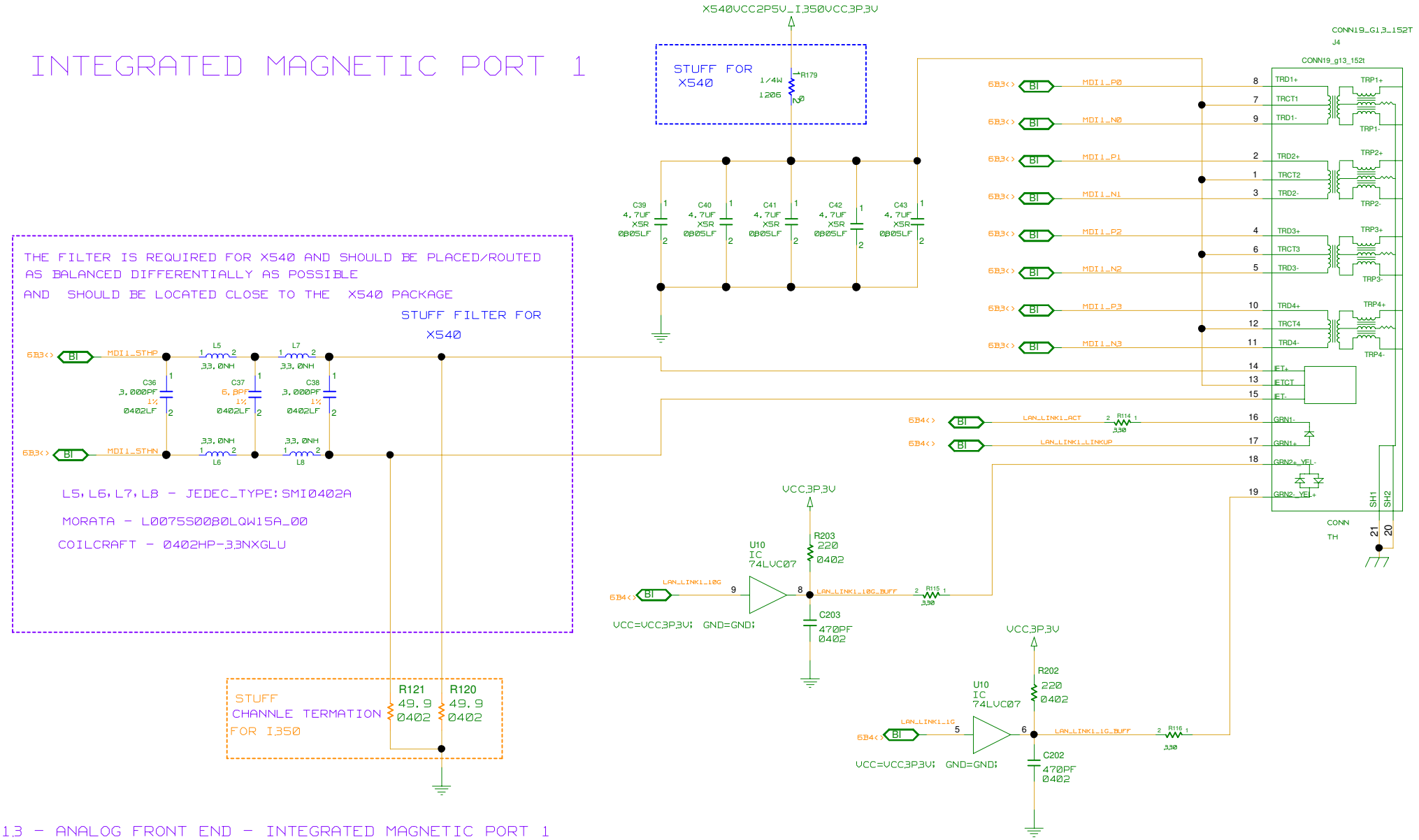
INTEGRATED MAGNETIC PORT 1



1.3 - ANALOG FRONT END - INTEGRATED MAGNETIC PORT 1

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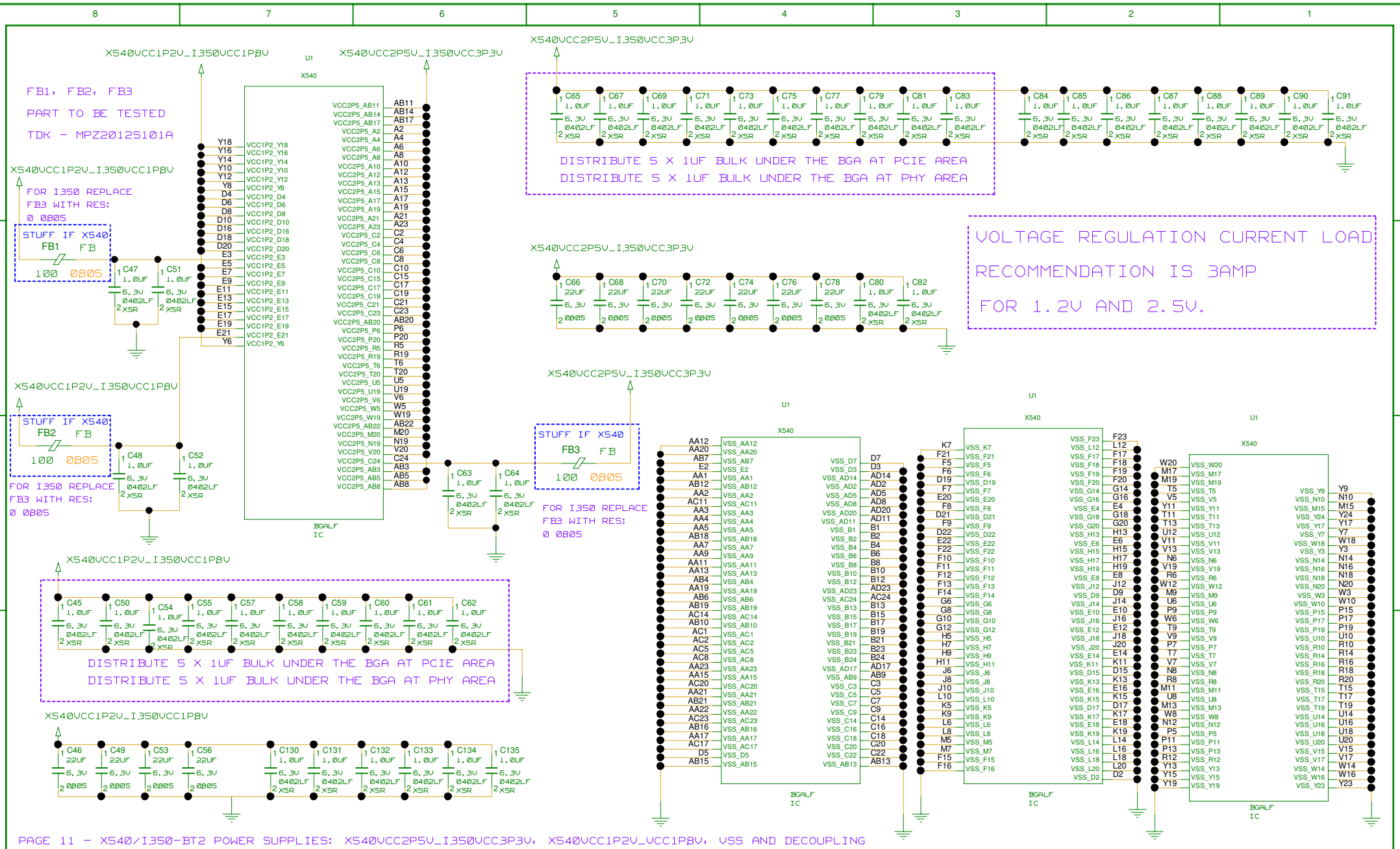
X540VCC1P2V_I,350VCC1P8V
X540VCC2P5V_I,350VCC,3P,3V
FB1, FB2, FB3
PART TO BE TESTED
TDK - MPZ2012S101A
FOR I350 REPLACE
FB3 WITH RES:
0 0805
STUFF IF X540
FB1 FB
100 0805
STUFF IF X540
FB2 FB
100 0805
STUFF IF X540
FB3 FB
100 0805
DISTRIBUTE 5 X 1UF BULK UNDER THE BGA AT PCIE AREA
DISTRIBUTE 5 X 1UF BULK UNDER THE BGA AT PHY AREA
VOLTAGE REGULATION CURRENT LOAD
RECOMMENDATION IS 3AMP
FOR 1.2V AND 2.5V.
X540
BGALF
IC
PAGE 11 - X540/I350-BT2 POWER SUPPLIES: X540VCC2P5V_I,350VCC,3P,3V, X540VCC1P2V_VCC1P8V, VSS AND DECOUPLING
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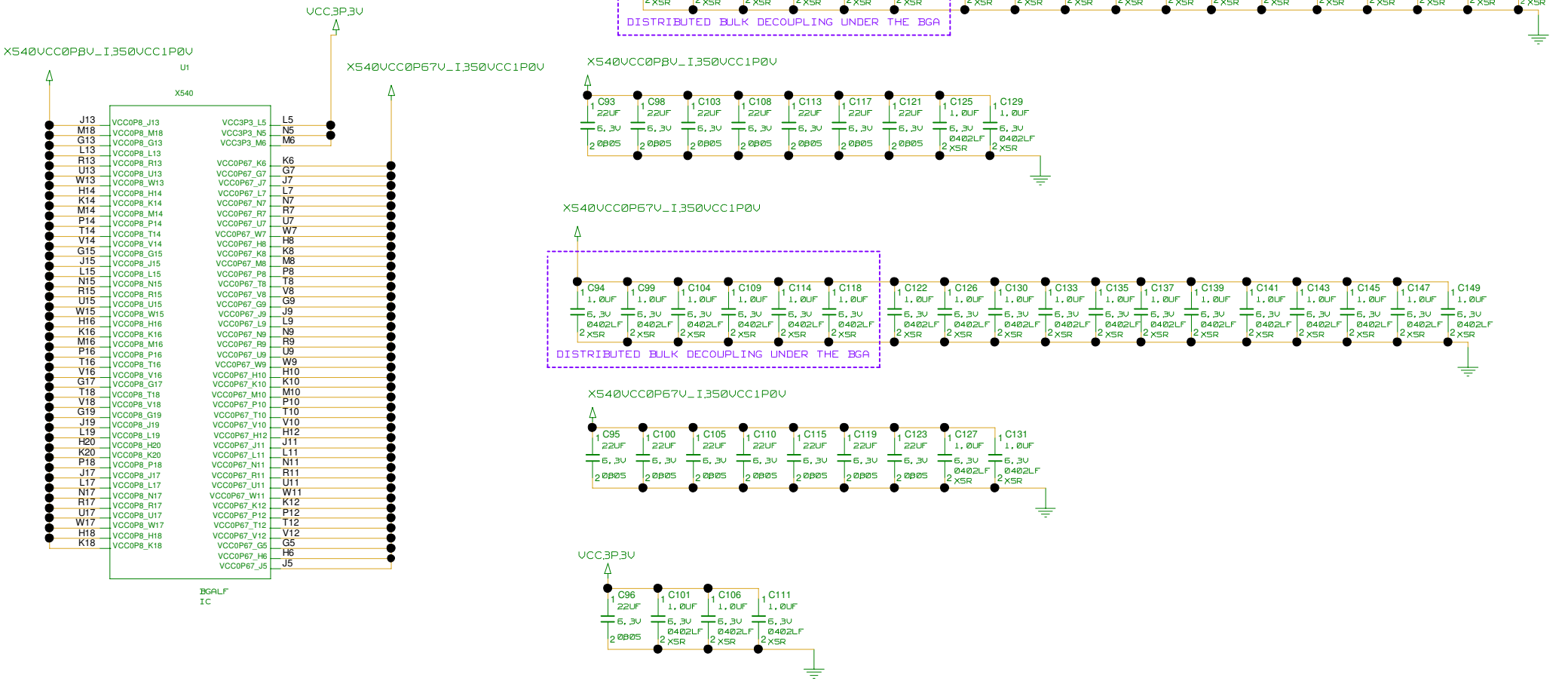
VOLTAGE REGULATION CURRENT LOAD

RECOMMENDATION IS 10AMP

FOR LVDD (0.65V) AND VDD (0.80V).



PAGE 12 - X540/I350-BT2 POWER SUPPLIES: X540VCC3P3V_I350VCC3P3, X540VCC0P8V_I350VCC1P0, X540VCC0P67V__I350VCC1P0 AND DECOUPLING

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE X540/I350-BT2 REFERENCE SCHEMATIC	SIZE B	CODE	DOCUMENT NUMBER	REV 2.1	DATE 11/27/2012	SHEET 12