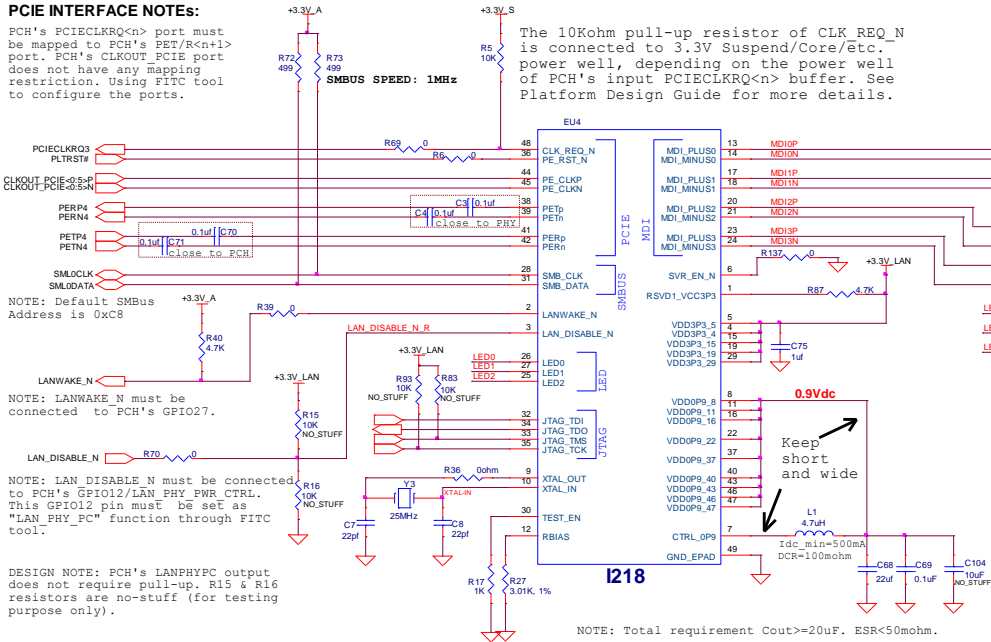


Intel® Ethernet Connection I218 Reference Schematic

March 2013 – Rev1.5
Copyright© Intel Corporation, 2013

PCIE INTERFACE NOTES:

PCH's PCIECLKREQ<n> port must be mapped to PCH's PET/R<n+1> port. PCH's CLKOUT_PCIE<n> port does not have any mapping restriction. Using FITC tool to configure the ports.



NOTE: Default SMBus Address is 0xc8

NOTE: LANWAKE_N must be connected to PCH's GPIO27.

NOTE: LAN_DISABLE_N must be connected to PCH's GPIO12/LAN_PHY_PWR_CTRL. This GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

DESIGN NOTE: PCH's LANPHYPC output does not require pull-up. R15 & R16 resistors are no-stuff (for testing purpose only).

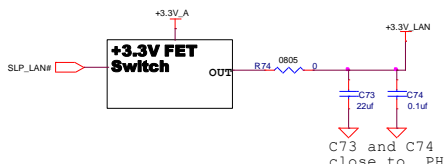
DESIGN NOTE: C7 & C8 value may vary depending on the actual Cstray of the board. Cstray is varied because specific board stack-up, layout, etc. For examples: Using Cload=18pF Crystal part, if Cstray=7pF then C7=C8=22pF and if Cstray=6pF then C7=C8=24pF. Cload=((C7+C8)/(C7+C8)) + Cstray. Each design should measure the crystal's ppm to make sure it is within the I218 Specification.

REVISION HISTORY

| Rev | Notes |
|-----|---|
| 1.0 | 1st release (based I217 Reference Schematic Rev1.7) *IMPORTANT NOTE: I218 only supports iSVM. See I218 documentation for details. |
| 1.5 | Update The Oscillator Circuit (only used if The Crystal Circuit is not in used) Update SMBUS, SLP_LAN#, and TVS notes. Update PCIE interface notes. |

The 10kOhm pull-up resistor of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKREQ<n> buffer. See Platform Design Guide for more details.

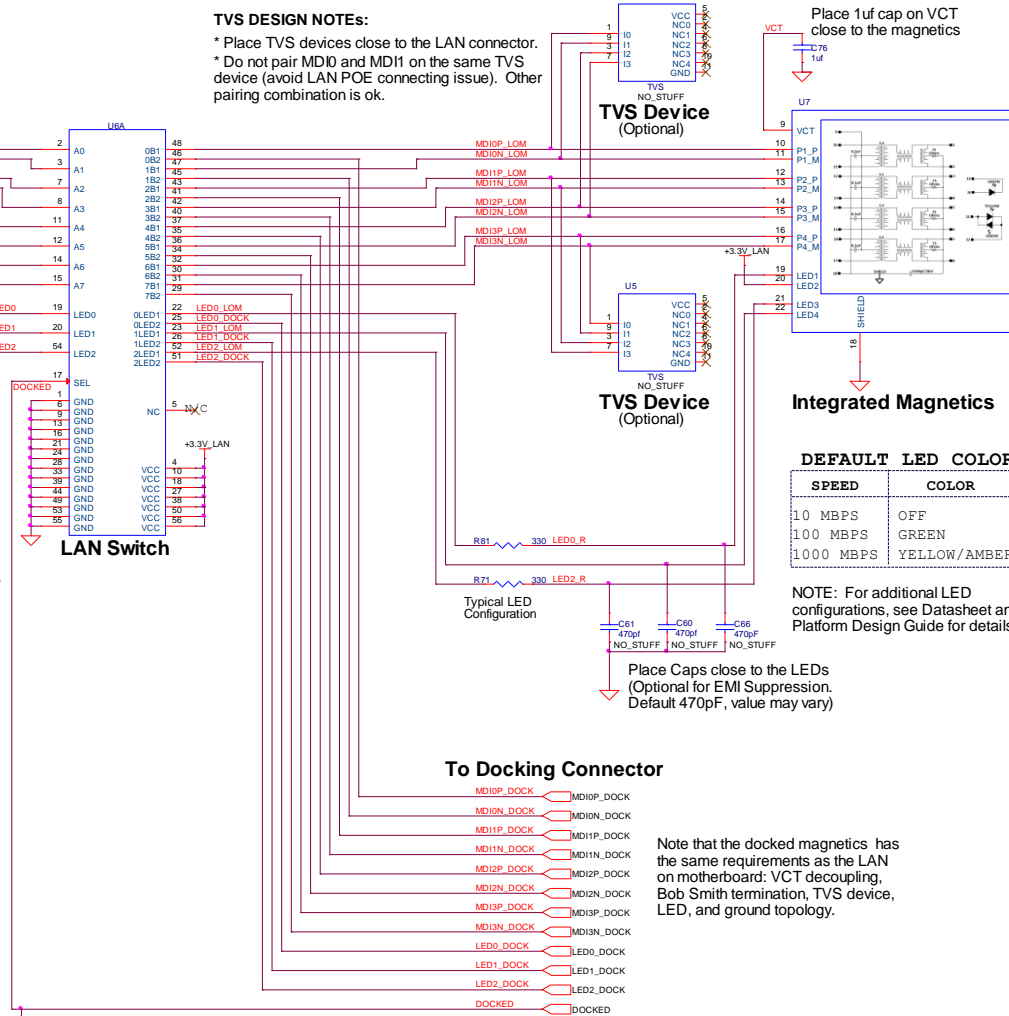
NOTE: Total requirement Cout>=20uF. ESR<50mohm. LAYOUT NOTE: Place L1, C68, C69, and C104 close to PHY



*IMPORTANT NOTE: PHY Power is controlled by SLP_LAN signal.

TVS DESIGN NOTES:

* Place TVS devices close to the LAN connector.
* Do not pair MD10 and MD11 on the same TVS device (avoid LAN POE connecting issue). Other pairing combination is ok.



Place 1uf cap on VCT close to the magnetics

Integrated Magnetics

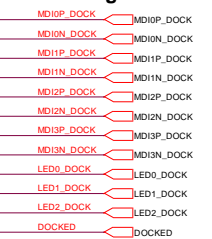
DEFAULT LED COLOR

| SPEED | COLOR |
|-----------|--------------|
| 10 MBPS | OFF |
| 100 MBPS | GREEN |
| 1000 MBPS | YELLOW/AMBER |

NOTE: For additional LED configurations, see Datasheet and Platform Design Guide for details.

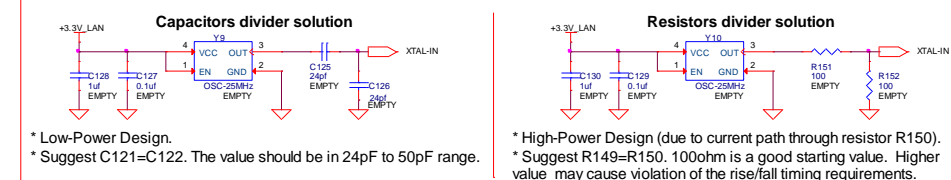
Place Caps close to the LEDs (Optional for EMI Suppression. Default 470pF, value may vary)

To Docking Connector



Note that the docked magnetics has the same requirements as the LAN on motherboard: VCT decoupling, Bob Smith termination, TVS device, LED, and ground topology.

OSCILLATOR DESIGN NOTE: Intel strongly suggests to use Crystal Circuit for i218 (widely use and low cost). However, it is also possible to design i218 with the Oscillator Solutions (to replace the Crystal Circuit). Below is 2 tested solutions.



* Low-Power Design.
* Suggest C121=C122. The value should be in 24pF to 50pF range.

* High-Power Design (due to current path through resistor R150).
* Suggest R149=R150. 100ohm is a good starting value. Higher value may cause violation of the rise/fall timing requirements.

NOTE: This is a typical Mobile Docking Design. For designs without a docking connector, the lanswitch device is not necessary so it can be removed. Please see the schematic/layout checklist for details.