The Intel® Multi Channel Video Processor is a highly configurable set of IP blocks and optional features that together provide a powerful range of tools for multi-video format conversion and image enhancement.

**Summary**

The Intel® Multi Channel Video Processor is a highly configurable set of IP blocks and optional features that together provide a powerful range of tools for multi-video format conversion and image enhancement for video formats up to 60Hz Ultra HD, with 120Hz Ultra HD output as a further option. For ease of implementation and to make best use of system resources, the principal IP blocks are packaged as a single OSVP core offering up to 8 video channels that you can individually configure to carry out the precise range of actions needed to deliver the transformations you require.

**Connectivity**

Omnitek provides a large range of complementary IP Cores for video processing and connection. These IP cores can be used individually or in combination to provide FPGA solutions for applications in broadcast, AV, aerospace/defence, medical and automotive industries. Omnitek can provide a bespoke solution which can be designed for you and tailored to your specific needs.
Key Features

Video Support:
- Interlaced, progressive or segmented frame (PsF) video input formats up to 4096 x 2160 at 60Hz
- Interlaced or progressive output Video output formats up to 4096 x 2160 at 120Hz
- YUV and RGB colour in 4:2:0, 4:2:2 or 4:4:4 format
- 8, 10 or 12-bit colour depths
- Up to 8 video processing paths, each individually configured for video standard and processing

Full 12-bit YUV or RGB 4:4:4 processing:
- Up/Down/Cross conversion between any supported standards
- Asynchronous input and output timing with frame synchronization (when changing frame rate)
- Chroma re-sampling
- Full 6-axis YUV/RGB colour correction, brightness and saturation level control, and hue rotation with Colour primary mapping
- Motion- and/or Edge-adaptive de-interlacing with best-in-class low-angle handling
- 3:2 and 2:2 film cadence detection and processing, including handling of mixed cadence such as interlaced video over 3:2 film
- Noise reduction
- Crop and resize with Super-Resolution image enhancement
- Alpha blending of multiple video sources

Design Environment:
- Resource use and signal timing optimised through packaging the main processing blocks as single configurable OSVP core
- AXI4-Stream interfaces for video; AXI4-MM to SDRAM controller; AXI4-Lite to control registers
- Omnitek FPGA Software Interface Framework for easy prototyping, with drivers for Linux and Windows that present identical APIs

Chroma Re-sampler

Chroma re-sampling may be needed both to up-sample the incoming video stream to the 4:4:4 format used for signal processing throughout the OSVP core and to deliver the required output video format.

The MCVP Suite includes 4:2:2 to 4:4:4 and 4:4:4 to 4:2:2 re-samplers as standard. 4:2:2 to 4:2:0 and 4:2:0 to 4:2:2 Chroma re-samplers are available as an add-on to the OSVP Suite. All four re-samplers may be used alongside the OSVP core or instantiated independently as required

Input De-Interlacer

Interlaced and PsF format inputs need to be de-interlaced prior to signal processing. However special care is needed in order to avoid generating artefacts, particularly where the video includes motion or low-angle edges. Failure to detect film cadences correctly will also give rise to artefacts in the de-interlaced video stream.

Figure 2. Simple line interpolation gives rise to jaggy artefacts and flickering static content.

Figure 3. With advanced low angle edge interpolation and motion detection, the jaggy artefacts are removed and static content is enhanced.

Motion-Adaptive De-interlacing and Low-Angle Edge Correction are provided as standard, but with the Advanced option, the OSVP benefits from the use of highly-sophisticated Low-angle Edge Detection and Film Cadence Processing algorithms.

The Film Cadence Processing is able to handle 3:2 and 2:2 file cadences for all types, together with mixed cadence material such as interlaced text overlaid on a 3:2 film cadence.

Figure 4. Failure to detect film cadences gives rise to spurious artefacts both in 2:2 cadence material (top) and 3:2 cadence material (bottom).

Figure 5. Responsive film cadence detection allows the original material to be recovered without artefacts.
Noise Reduction

Before an image is up-sized, it is advisable to remove any noise or stuck pixels. The OSVP Suite Advanced option adds Noise Reduction to the range of facilities offered by the OSVP core. Noise is reduced by applying a variable statistical filter to the signal. This approach achieves good results with both specular noise and stuck pixels.

Colour Space Conversion and Colour Primaries

A necessary part of transforming video is the mapping of pixel data between colour spaces in order to preserve the colouring of the content. This mapping is required because the different formats define different sets of primary colours. For example, SD uses the Rec 601 set of colour primaries, while HD follows Rec 709 and UHD follows Rec 2020. Each display device also uses a particular set of primary colours.

The marked difference between the colour spaces used by these standards is illustrated below. The two triangles formed by joining the Colour Primaries for HD (Rec 709) and UHD (Rec 2020) enclose the colour spaces defined for these two formats.

The OSVP Colour Space Conversion block enables pixel data to be transformed between any input colour space and any output colour space. All that is needed is the three primary colours and the white point associated with each colour space. The colour spaces need to be accurately defined: any errors in their definition will result in a poor colouration.

The OSVP Colour Conversion block supports standard colour spaces such as those defined for SD, HD and UHD. With the Advanced option, it also supports user-defined colour spaces, allowing detailing of the colour space used by a particular display device. It also offers gamma correction, allowing the correction of any gamma that may have been applied.

The OSVP Colour Correction block offers the flexibility of mapping between input and output gamma curves.

6 Axis Colour Correction allows you to make both RGB and YUV lift and gain adjustments.

Brightness, Saturation and Hue can be used to swap colours and enhance their presence.

They can also be used to simulate photographic effects such as sepia-toning.
Image Re-sizer

Moving between different resolutions and compositing several source images into a single image typically requires images to be resized. The OSVP Re-sizer allows images to be compressed or expanded across the full range of image resolutions. Moreover the technique used makes highly efficient use of the underlying FPGA/SoCs DSP resources.

The process of resizing an image is however prone to introducing a range of unwanted effects. For instance, the result of up-scaling an image often appears softened. Another common effect is ringing near edges.

The Combiner allows up to 16 channels to be combined into a single video frame, with the user specifying the X,Y position and the transparency of that image and which layer it occupies.

Frame Synchronizer

Differences between the input and output frame rate are handled by Frame Sync logic within the OSVP core that repeats frames or drop frames as required.

Output Interlacer

To allow video to be output in Interlaced formats, the OSVP suite also includes an Interlacer block that can be instantiated alongside the OSVP core where Interlaced output is required.

Connectivity

The OSVP core and other blocks of the OSVP Suite all offer AXI4 interfacing: AXI4-S stream interfacing for video, AXI4-Lite interfacing for control and AXI4-MM for memory management.

Image resizing and de-interlacing involve reading and writing to SDRAM. Processing multiple channels requires multiple SDRAM accesses, together with the necessary logic to arbitrate the different operations. This logic is built into the OSVP core and is presented as a single AXI4-MM interface.

Adding the Advanced option to the MCVP adds a range of Super-Resolution Enhancement algorithms that both counteract these effects and offer different levels of smoothness or sharpening in the end result.

Image Combiner

As well as providing the facility to process more than one video stream at a time, the OSVP also includes a Combiner block that can be instantiated to pull the output from OSVP video channels together into a single final image.
Product Options
OSVP_SUITE: OSVP core offering 1 – 8 channels of up to 1080p resolution. Comprises Chroma re-samplers, colour matrix, de-interlacer, crop, re-size, frame synchronization, Combiner and Interlacer blocks.

OSVP_ADV: Adds support for up to 4K60 Ultra HD. Also adds 6-axis colour correction, noise reduction, super-resolution image enhancement, enhanced cadence detection and low-angle de-interlacing.

OSVP_120: Adds support for output frame rates up to 120Hz.

OSVP_4:2:0: Adds 4:2:2 to 4:2:0 and 4:2:0 to 4:2:2 Chroma re-samplers.

2D_GRAPHICS: Adds an OS frame buffer and 2D acceleration.

SDI: Adds SD up to 12G-SDI I/O connectivity.

HDMI2.0: Adds HDMI I/O connectivity.

DP1.2: Adds DisplayPort I/O connectivity.

8K Option: provides support for 7680×4320 image at 120Hz

Software Support
The OSVP Suite IP includes drivers, kernel mode code and other supporting software to allow the development of applications within Omnitek's FPGA Software Interface Framework. This makes prototyping easy by using the same API to access FPGA IP facilities across different operating systems (Linux or Windows) and different hardware.

This removes the need to write any Kernel Mode code and allows the same source code to be used across compatible but distinct implementations of any system.

Design Your Product Today with Intel FPGAs
Intel provides a large range of complementary and modular in-house IP cores for video processing and connectivity. These IP cores can be used to create complete solutions for applications in Broadcast, ProAV, Aerospace/Defense, Medical, Automotive and more.

You can get more information on available video IP at www.intel.com/fpga-broadcast or contact an Intel sales representative for further inquiries.

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