

Audio Embed/Extract FPGA IP

Intel® provide an SDI Audio Extractor IP Core and an SDI Audio Embedder IP Core.

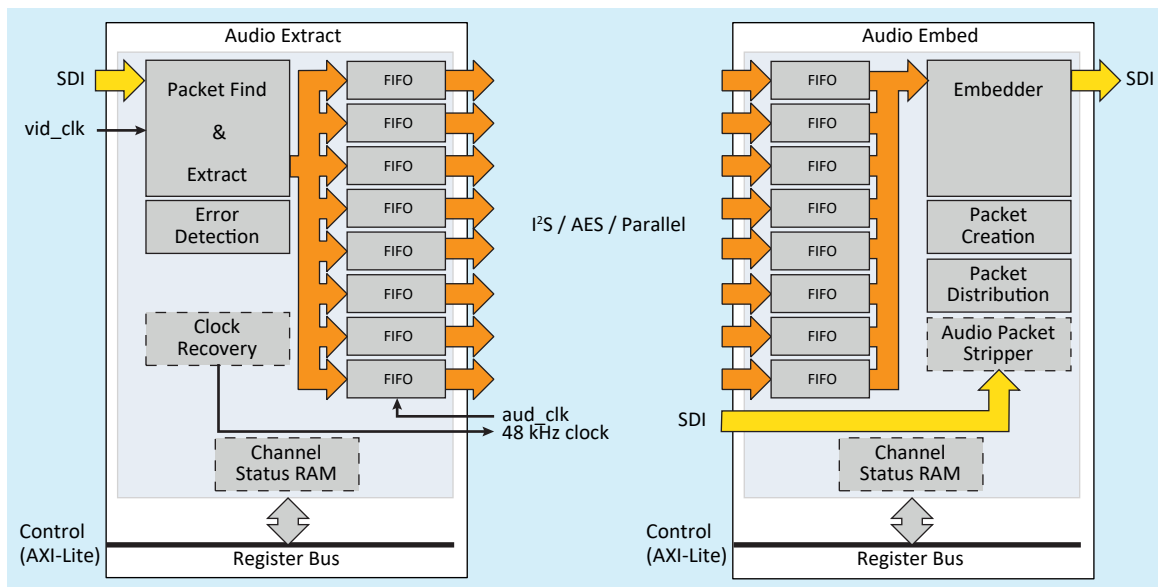


Figure 1. Functional block diagram of the Audio Embed/Extract IP

Summary

Intel® provide an SDI Audio Extractor IP Core and a SDI Audio Embedder IP Core.

The SDI Audio Extractor block is designed to extract audio delivered as SMPTE 272M packed data from SD-SDI and audio delivered as SMPTE 299M packed data from HD-SDI. The extracted audio may be output in either I2S Audio, AES Audio, or Parallel Audio format.

The Embed block allows audio to be embedded in up to 16 channels (8 channel pairs). The Extract block is designed to extract audio from a single channel pair but multiple blocks may be used together to extract the audio from

multiple channel pairs.

The audio embedded by the SDI Audio Embedder IP Core is formatted either in accordance with the SMPTE 272M standard (for SD video) or in accordance with the SMPTE 299M standard (for HD and for 3G video).

The input audio may be at any of the sample rates permitted by the above SMPTE standards and can be provided in either I2S Audio, AES Audio or Parallel Audio format. It can also be either synchronous or asynchronous to the video.

Operations in both IP Cores are setup with using registered accessed via the Register Bus.

Applications

The Intel SDI Audio Extractor and SDI Audio Embedder IP Cores can be used in a range of applications including:

- SDI audio embedding and extraction
- SDI audio editing
- SDI audio monitoring and analysis

Key Features

- Audio Embed/Extract firmware
- Handle audio conforming to SMPTE 272M (SD) or SMPTE 299M (HD/3G), presented as I2S Audio, AES Audio or Parallel Audio
- Support all sample rates permitted by the SMPTE standards
- SDI Audio Embedder IP Core handles up to 16 channels (8 channel pairs); Extract block handles one channel pair but multiple blocks can be used together to handle the required number of channels
- Embed Block able to strip out existing audio
- SDI Audio Embedder IP Core includes sine generator for test purposes
- Information reported by Extract Block includes which audio groups and control packets have been detected, a decode of the Audio Control Packet; and ancillary packet checksum, parity field and CRC error counts
- Both blocks controlled through set of slave registers accessed either through exposed ports or via optional register interface block
- Both blocks optionally available as source code in either Verilog or VHDL.



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